AMRITASAI INSTITUTE OF SCIENCE AND TECHNOLOGY PARITALA, 521180

AR22 REGULATION

COURSE STRUCTURE AND SYLLABUS

B.Tech ELECTRONICS & COMMUNICATION ENGINEERING

(VLSI DESIGN & TECHNOLOGY)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Amrita Sai Institute of Science & Technology

(AN AUTONOMOUS INSTITUTION)

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK Kakinada)
AN ISO 9001: 2015 Certified Institution, Accredited by NAAC ,
Recognized by UGC Under 2(f) and 12(B) under UGC act 1956
Parital, Kanchikacherla (M), NTR Dist., A.P., India-521180
www.amritasai.org.in Tel:08678-277777 Toll Free No: 1800 1212 369

DEPARTMENT OF ELECTRONICS and COMMUICATION ENGINEERING

INSTITUTION VISION

Contribute significantly to Technology and Management for transforming the lives of individuals and society through continuous Innovation in Technical Education, Research and Entrepreneurship.

INSTITUTION MISSION

To enrich the students to play key role in Technology and Management globally through best in class innovative methodologies developing critical thinking and problem solving, research and Entrepreneurship.

DEPARTMENT VISION

To create efficient engineers proficient with the domains related to Electronics and Communications engineering for a successful career in the service of society.

DEPARTMENT MISSION

To be able to develop sustainable solutions to problems related to Electronics and Communications Engineering as an individual or as a part of a team to maintain professional ethics, experimental learning, collaborations for research and Entrepreneurship.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: To Acquire a strong background in basic science and mathematics and the ability to use these tools in Electronics & Communications Engineering.

PEO2: To develop the ability to demonstrate technical competence and develop solutions to the problems in various fields of Electronics & Communications Engineering.

PEO3: To produce graduates who ensure ethical and moral behavior.

PROGRAM SPECIFIC OUTCOMES (PSO'S)

PROFESSIONAL COMPETANCE: Apply the knowledge of Electronics and Communication Engineering principles in different domains like VLSI, Signal Processing, Communication, and Embedded Systems.

TECHNICAL SKILLS: Able to design and implement products using the state of art hardware and software tools and hence provide simple solutions to complex problems.

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PROGRAM OUTCOMES

PO1 Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 Design/Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of engineering practice.

PO9 Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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ACCREDITED BY NAAC WITH "A" GRADE

PARITALA(P), KANCHIKACHERLA(M), KRISHNA (D)-521 180(A. P.)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE STRUCTURE FOR AR-22 REGULATION

I YEAR I SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22HS1T1	COMMUNICATIVE ENGLISH-I	HSC	3	0	0	**3**
2	22BS1T2	ALGEBRA & DIFFERENTIAL EQUATION	BSC	3	0	0	**3**
3	22BS1T3	ENGINEERING PHYSICS	BSC	3	0	0	**3**
4	22ES1T4	C PROGRAMMING	ESC	3	0	0	**3**
5	22ES1T5	BASICS OF ENGINEERING AND TECHNOLOGY	ESC	1	0	4	**3**
6	22HS1L1	COMMUNICATIVE ENGLISH LAB-I	HSL	0	0	3	**1.5**
7	22BS1L2	ENGINEERING PHYSICS & WORKSHOP LAB	BSL	0	0	3	**1.5**
8	22ES1L3	C PROGRAMMING LAB	ESL	0	0	3	**1.5**
9	22ES1MC1	LEARNING AN ART FORM	MC	2	0	0	0
TOTAL CREDITS							**19.5**

I YEAR II SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22HS2T1	COMMUNICATIVE ENGLISH-II	HSS	3	0	0	**3**
2	22BS2T2	CALCULAS AND TRANSFORMATIONS	BSC	3	0	0	**3**
3	22BS2T3	ENGINEERING CHEMISTRY	BSC	3	0	0	**3**
4	22ES2T4	PYTHON PROGRAMMING	ESC	3	0	0	**3**
5	22ES2T5	BASICS OF IOT	ESC	1	0	4	**3**
6	22HS2L1	COMMUNICATIVE ENGLISH LAB-II	HSL	0	0	3	**1.5**
7	22BS2L2	ENGINEERING CHEMISTRY & ITWS LAB	BSL	0	0	3	**1.5**
8	22ES2L3	PYTHON PROGRAMMING LAB	ESL	0	0	3	**1.5**
9	22ES2MC1	ENVIRONMENTAL STUDIES	MC	2	0	0	0
TOTAL CREDITS							**19.5**

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Proceedings of the 1st meeting of Board of Studies in Electronics and Communication Engineering held on 18/07/2025 at 1:30 PM in Online, Amrita Sai Institute of Science and Technology, Paritala.

S. No.	Member	Signature	S. No.	Member	Signature
1	**Dr. V. Ramesh Babu** Professor & Head, Department of ECE, ASIST, Paritala		2	**Dr. A.M.Prasad** Professor, Department of ECE, JNTU, Kakinada	
3	**Dr. B. Rajendra Naik** Professor, Department of ECE, Osmania University, Hyderabad		4	**Dr. Habibulla Khan** Professor, Department of ECE, KL University, Vijayawada	
5	**Mr. V. Govinda Rao** CEO, Microlink Information Technologies Vijayawada		6	**Dr. Samiran Chatterjee** Professor, Department of ECE, ASIST, Paritala	
7	**Dr. A. Vijayalakshmi** Professor, Department of ECE, ASIST, Paritala		8	**Dr. D. Hema** Associate Professor, Department of ECE, ASIST, Paritala	
9	**Mr. Abdul Azeez** Assistant Professor, Department of ECE, ASIST, Paritala		10	**Mrs. N. Thirumalesh** Assistant Professor, Department of ECE, ASIST, Paritala	
11	**Mr. B. Rama Rao** Associate Professor, Department of ECE, ASIST, Paritala		12	**Mr. B. Balaji** Associate Professor, Department of ECE, ASIST, Paritala	
13	**Mr. Anurag Sharma** Assistant Professor, Department of ECE, ASIST, Paritala		14	**Mrs. G. Latha** Assistant Professor, Department of ECE, ASIST, Paritala	
15	**Mrs. N. Visranthamma** Assistant Professor, Department of ECE, ASIST, Paritala		16	**Mrs. Ch. Sreelakshmi** Assistant Professor, Department of ECE, ASIST, Paritala	
17	**Mrs. V. Swarnalatha** Assistant Professor, Department of ECE, ASIST, Paritala		18	**Mrs. B. Suneetha** Assistant Professor, Department of ECE, ASIST, Paritala	
19	**Mrs. M. Saraswathi** Assistant Professor, Department of ECE, ASIST, Paritala		20	**Mrs. T. Venkata Ramana** Assistant Professor, Department of ECE, ASIST, Paritala	
21	**Mr. Md. Faheem** Assistant Professor, Department of ECE, ASIST, Paritala		22	**Mr. Sd. Nagura Vali** Technical Assistant, Department of ECE, ASIST, Paritala	
23	**Mr. P. Srinivasa Rao** Technical Assistant, Department of ECE, ASIST, Paritala				
Special Invitees					
26	**Dr. P. Chiranjeevi** Professor & Director of Academics, Department of CSE ASIST, Paritala				

At the outset, the Chairperson, BOS in Electronics and Communication Engineering, welcomed all members of Board of Studies and Special invitees present in the meeting of Board of Studies for 2025-26 admitted batch in Department of Electronics and Communication Engineering and briefed about the agenda to be discussed. The following agenda was placed by the Chairperson and decisions were taken after detailed deliberations.

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Proceedings of the 4th meeting of Board of Studies in Electronics and Communication Engineering- VLSI Design and Technology (EVT) held on 17/07/2025 at 10:30 AM in Online, Amrita Sai Institute of Science and Technology, Paritala.

S. No.	Member	Signature	S. No.	Member	Signature
1	**Dr. V. Ramesh Babu** Professor & Head, Department of ECE, ASIST, Paritala		2	**Dr. A.M.Prasad** Professor, Department of ECE, JNTU, Kakinada	
3	**Dr. B. Rajendra Naik** Professor, Department of ECE, Osmania University, Hyderabad		4	**Dr. Habibulla Khan** Professor, Department of ECE, KL University, Vijayawada	
5	**Mr. V. Govinda Rao** CEO, Microlink Information Technologies Vijayawada		6	**Dr. Samiran Chatterjee** Professor, Department of ECE, ASIST, Paritala	
7	**Dr. A. Vijayalakshmi** Professor, Department of ECE, ASIST, Paritala		8	**Dr. D. Hema** Associate Professor, Department of ECE, ASIST, Paritala	
9	**Mr. Abdul Azeez** Assistant Professor, Department of ECE, ASIST, Paritala		10	**Mrs. N. Thirumalesh** Assistant Professor, Department of ECE, ASIST, Paritala	
11	**Mr. B. Rama Rao** Associate Professor, Department of ECE, ASIST, Paritala		12	**Mr. B. Balaji** Associate Professor, Department of ECE, ASIST, Paritala	
13	**Mr. Anurag Sharma** Assistant Professor, Department of ECE, ASIST, Paritala		14	**Mrs. G. Latha** Assistant Professor, Department of ECE, ASIST, Paritala	
15	**Mrs. N. Visranthamma** Assistant Professor, Department of ECE, ASIST, Paritala		16	**Mrs. Ch. Sreelakshmi** Assistant Professor, Department of ECE, ASIST, Paritala	
17	**Mrs. V. Swarnalatha** Assistant Professor, Department of ECE, ASIST, Paritala		18	**Mrs. B. Suneetha** Assistant Professor, Department of ECE, ASIST, Paritala	
19	**Mrs. M. Saraswathi** Assistant Professor, Department of ECE, ASIST, Paritala		20	**Mrs. T. Venkata Ramana** Assistant Professor, Department of ECE, ASIST, Paritala	
21	**Mr. Md. Faheem** Assistant Professor, Department of ECE, ASIST, Paritala		22	**Mr. Sd. Nagura Vali** Technical Assistant, Department of ECE, ASIST, Paritala	
23	**Mr. P. Srinivasa Rao** Technical Assistant, Department of ECE, ASIST, Paritala				
Special Invitees					
26	**Dr. P. Chiranjeevi** Professor & Director of Academics, Department of CSE ASIST, Paritala				

At the outset, the Chairperson, BOS in Electronics and Communication Engineering- VLSI Design and Technology (EVT), welcomed all members of Board of Studies and Special invitees present in the meeting of Board of Studies for 2024-25 admitted batch in Department of Electronics and Communication Engineering and briefed about the agenda to be discussed. The following agenda was placed by the Chairperson and decisions were taken after detailed deliberations.

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Proceedings of the 4th meeting of Board of Studies in Electronics and Communication Engineering- Advanced Communication Technology (ECA) held on 17/07/2025 at 10:30 AM in Online, Amrita Sai Institute of Science and Technology, Paritala.

S. No.	Member	Signature	S. No.	Member	Signature
1	**Dr. V. Ramesh Babu** Professor & Head, Department of ECE, ASIST, Paritala		2	**Dr. A.M.Prasad** Professor, Department of ECE, JNTU, Kakinada	
3	**Dr. B. Rajendra Naik** Professor, Department of ECE, Osmania University, Hyderabad		4	**Dr. Habibulla Khan** Professor, Department of ECE, KL University, Vijayawada	
5	**Mr. V. Govinda Rao** CEO, Microlink Information Technologies Vijayawada		6	**Dr. Samiran Chatterjee** Professor, Department of ECE, ASIST, Paritala	
7	**Dr. A. Vijayalakshmi** Professor, Department of ECE, ASIST, Paritala		8	**Dr. D. Hema** Associate Professor, Department of ECE, ASIST, Paritala	
9	**Mr. Abdul Azeez** Assistant Professor, Department of ECE, ASIST, Paritala		10	**Mrs. N. Thirumalesh** Assistant Professor, Department of ECE, ASIST, Paritala	
11	**Mr. B. Rama Rao** Associate Professor, Department of ECE, ASIST, Paritala		12	**Mr. B. Balaji** Associate Professor, Department of ECE, ASIST, Paritala	
13	**Mr. Anurag Sharma** Assistant Professor, Department of ECE, ASIST, Paritala		14	**Mrs. G. Latha** Assistant Professor, Department of ECE, ASIST, Paritala	
15	**Mrs. N. Visranthamma** Assistant Professor, Department of ECE, ASIST, Paritala		16	**Mrs. Ch. Sreelakshmi** Assistant Professor, Department of ECE, ASIST, Paritala	
17	**Mrs. V. Swarnalatha** Assistant Professor, Department of ECE, ASIST, Paritala		18	**Mrs. B. Suneetha** Assistant Professor, Department of ECE, ASIST, Paritala	
19	**Mrs. M. Saraswathi** Assistant Professor, Department of ECE, ASIST, Paritala		20	**Mrs. T. Venkata Ramana** Assistant Professor, Department of ECE, ASIST, Paritala	
21	**Mr. Md. Faheem** Assistant Professor, Department of ECE, ASIST, Paritala		22	**Mr. Sd. Nagura Vali** Technical Assistant, Department of ECE, ASIST, Paritala	
23	**Mr. P. Srinivasa Rao** Technical Assistant, Department of ECE, ASIST, Paritala				
Special Invitees					
26	**Dr. P. Chiranjeevi** Professor & Director of Academics, Department of CSE ASIST, Paritala				

At the outset, the Chairperson, BOS in Electronics and Communication Engineering- Advanced Communication Technology (ECA), welcomed all members of Board of Studies and Special invitees present in the meeting of Board of Studies for 2024-25 admitted batch in Department of Electronics and Communication Engineering and briefed about the agenda to be discussed. The following agenda was placed by the Chairperson and decisions were taken after detailed deliberations.

The Chairman of the Board of Studies (BoS) in Electronics and Communication Engineering welcomed members and special invitees, briefed on the meeting's agenda, and led discussions on key topics, resulting in decisions being made after detailed deliberations:

The Agenda for the Meeting:

1. Review of ECE/EVT/ECA course structure for AR-22 regulation
2. Suggestions on preparation of M. Tech course structure for AR-25 regulation.
3. Suggestions on preparation of B. Tech course structure for AR-23 regulation.

Agenda 1: Review of ECE/EVT/ECA course structure for AR-22 regulation

The Chairman appraised the members about the Autonomous syllabus with total credit points for Electronics and Communication Engineering to obtain B.Tech degree for ECE and ECE-allied branch. The Chairman is discussing:

1. Autonomous syllabus for Electronics and Communication Engineering (ECE)
2. Total credit points required for B.Tech degree in ECE and ECE-allied branches
3. AR-22 course structure for review and approval

Resolution: The Board of Studies (BoS) went through the course structure and discussed about the opinion given in the 1st BoS proceedings has:

1. Reviewed the AR-22 course structure for ECE and ECE-allied branches
2. Discussed and incorporated feedback from previous meetings
3. Approved the course structure for 3rd year to final year (5th sem-8th sem)

Attachment: Annexure-I

Agenda 2: Suggestions on preparation of M. Tech course structure for AR-25 regulation

The Chairman has presented the M.Tech course structure under the AR-25 regulation for academic year 2025-26 admitted batch:

1. Review 2. Discussion 3. Approval

The board will provide their opinions and feedback before approving the course structure.

Resolution: The Board of Studies (BoS) went through the course structure and shared their opinion given below:

1. Reviewed the course syllabus
2. Incorporated suggested changes
3. Approved the M. Tech course structure & syllabus.

This approval finalizes the AR-25 curriculum for the M.Tech program for academic year 2025-26 admitted batch.

Attachment: Annexure-II

Agenda 3: Suggestions on preparation of B. Tech course structure for AR-23 regulation

The Chairman has presented the B.Tech course structure under the AR-23 regulation for academic year 2025-26 admitted batch

1. Review 2. Discussion 3. Approval

The board will provide their opinions and feedback before approving the course structure.

Resolution: The Board of Studies (BoS) went through the course structure and shared their opinion given below:

1. Reviewed the course syllabus
2. Incorporated suggested changes
3. Approved the B. Tech course structure & syllabus.

This approval finalizes the AR-23 curriculum for the B.Tech program for academic year 2025-26 admitted batch.

Attachment: Annexure-III

Any other agenda

1. JNTUK expert member of BoS suggested that to follow the university curriculum and syllabus.
2. JNTUK expert member of BoS suggested the text books and reference books write as per the IEEE format.
3. Conduct Quizzes, Seminars, Guest Lectures to improve or impart extra knowledge amongst the students.
4. Suggested to include Honours subject.

There being no other agenda, the meeting was ended with a vote of thanks to the chair.

Dr. V. RAMESH BABU
Professor & Head of the Department,
BoS Chairman,
Department of ECE,
ASIST, Paritala

II YEAR I SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22BS3T1	NUMERICAL METHODS AND COMPLEX VARIABLES	BSC	3	0	0	**3**
2	22EC3T2	SWITCHING THEORY AND LOGIC DESIGN	PCC	3	0	0	**3**
3	22EC3T3	ELECTRONIC DEVICES AND CIRCUITS	PCC	3	0	0	**3**
4	22EA3T4	CIRCUIT THEORY	PCC	3	0	0	**3**
5	22EV3T5	PRINCIPLES OF COMMUNICATION	PCC	3	0	0	**3**
6	22EC3L1	SWITCHING THEORY AND LOGIC DESIGN LAB	PCC	0	0	3	**1.5**
7	22EC3L2	ELECTRONIC DEVICES AND CIRCUITS LAB	PCC	0	0	3	**1.5**
8	22EV3L3	COMMUNICATIONS LAB	PCC	0	0	3	**1.5**
9	22HS3S1	ADVANCED ENGLISH COMMUNICATION TRAINING	SOC	1	0	2	**2**
10	22EC3MC1	INDIAN TRADITIONAL KNOWLEDGE	MC	2	0	0	**0**
TOTAL CREDITS							**21.5**

II YEAR II SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22BS4T1	PROBABILITY AND STATISTICS	BSC	3	0	0	**3**
2	22EV4T2	CMOS ANALOG IC DESIGN	PCC	3	0	0	**3**
3	22ET4T3	DIGITAL SIGNAL PROCESSING	PCC	3	0	0	**3**
4	22EV4T4	COMPUTER ARCHITECTURE	PCC	3	0	0	**3**
5	22EV4T5	DIGITAL SYSTEM DESIGN THROUGH VERILOG	PCC	3	0	0	**3**
6	22EV4L1	CMOS ANALOG IC DESIGN LAB	PCC	0	0	3	**1.5**
7	22ET4L2	DIGITAL SIGNAL PROCESSING LAB	PCC	0	0	3	**1.5**
8	22EV4L3	DIGITAL SYSTEM DESIGN THROUGH VERILOG LAB	PCC	0	0	3	**1.5**
9	22EC4S1	MINI PROJECT ON MATLAB PROGRAMMING WITH PCB DESIGN	SOC	1	0	2	**2**
TOTAL CREDITS							**21.5**
Honors/Minor courses (The hours distribution can be 3-0-2 or 3-1-0 also)							**4**
INTERNSHIP 4 TO 8 WEEKS (MANDATORY) DURING SUMMER VACATION							

III YEAR I SEMESTER							
SNO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22ET5T1	MICROPROCESSORS AND MICROCONTROLLERS	PCC	3	0	0	**3**
2	22EV5T2	DESIGN FOR TESTABILITY	PCC	3	0	0	**3**
3	22EC5T3	VLSI DESIGN	PCC	3	0	0	**3**
4		**PROFESSIONAL ELECTIVE COURSE -1/(SWAYAM)**	PEC	3	0	0	**3**
5		**OPEN ELECTIVE COURSE -1/(SWAYAM)**	OEC	3	0	0	**3**
6	22ET5L1	MICROPROCESSORS AND MICROCONTROLLERS LAB	PCC	0	0	3	**1.5**
7	22EV5L2	VLSI FRONT END LAB	PCC	0	0	3	**1.5**
8	22EC5S1	VERBAL, QUANTITATIVE AND REASONING TESTING	SOC	1	0	2	**2**
9	22EC5MC1	CONSTITUTION OF INDIA	MC	2	0	0	**0**
Summer Internship 4 to 8 weeks (Mandatory) after **Second Year** (to be evaluated during V semester)				0	0	0	**1.5**
TOTAL CREDITS							**21.5**
Honors/Minor courses (The hours distribution can be 3-0-2 or 3-1-0 also)							**4**

III YEAR II SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22EV6T1	LOW POWER VLSI DESIGN	PCC	3	0	0	**3**
2	22EV6T2	EMBEDDED SYSTEMS	PCC	3	0	0	**3**
3	22EV6T3	CMOS MIXED SIGNAL CIRCUIT DESIGN	PCC	3	0	0	**3**
4		**PROFESSIONAL ELECTIVE COURSE -2/(SWAYAM)**	PEC	3	0	0	**3**
5		**OPEN ELECTIVE COURSE -2/(SWAYAM)**	OEC	2	0	2	**3**
6	22EV6L1	VLSI BACK END LAB	PCC	0	0	3	**1.5**
7	22EV6L2	MIXED SIGNAL CIRCUIT DESIGN LAB	PCC	0	0	3	**1.5**
8	22EV6L3	IOT PROGRAMMING LAB	PCC	0	0	3	**1.5**
9	22EC6S1	CODING AND TECHNICAL TRAINING	SOC	1	0	2	**2**
							21.5
Honors/Minor courses (The hours distribution can be 3-0-2 or 3-1-0 also)							**4**
INTERNSHIP 4 TO 8 WEEKS (MANDATORY) DURING SUMMER VACATION							

IV YEAR I SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1		**PROFESSIONAL ELECTIVE COURSE -3 / (SWAYAM)**	PEC	3	0	0	**3**
2		**PROFESSIONAL ELECTIVE COURSE -4 / (SWAYAM)**	PEC	3	0	0	**3**
3		**PROFESSIONAL ELECTIVE COURSE -5 / (SWAYAM)**	PEC	3	0	0	**3**
4		**OPEN ELECTIVE COURSE -3 / (SWAYAM)**	OEC	2	0	2	**3**
5		**OPEN ELECTIVE COURSE -4 / (SWAYAM)**	OEC	2	0	2	**3**
6	22HS7T6	HUMANITIES AND SOCIAL SCIENCE ELECTIVE	HSC	2	0	0	**3**
7	22EC7S1	COMMUNITY BASED PROJECT	SOC	0	0	2	**2**
Industrial / Research Internship 4 to 8 WEEKS (Mandatory) after **Third Year** (to be evaluated during VII semester)					0	3	**3**
TOTAL CREDITS							**23**
Honors/Minor courses (The hours distribution can be 3-0-2 or 3-1-0 also)							**4**

IV YEAR II SEMESTER							
S NO	**CODE**	**COURSE TITLE**	**CATEGORY**	**L**	**T**	**P**	**C**
1	22EC8P1	MAJOR PROJECT/INTERNSHIP	PROJECT	0	0	0	**12**
TOTAL CREDITS							**12**

PROFESSIONAL ELECTIVE COURSES		**OPEN ELECTIVE COURSES**		**HUMANITIES AND SOCIAL SCIENCE ELECTIVE COURSES**	
1	MEMORY DEVICE CIRCUITS	**1**	COMPUTER NETWORKS	**1**	HUMAN RESOURCE DEVELOPMENT
2	DIGITAL IMAGE AND VIDEO PROCESSING	**2**	INDUSTRIAL ROBOTICS	**2**	IPR & PATENTS
3	GLOBAL POSITIONING SYSTEM	**3**	CLOUD COMPUTING	**3**	ADVANCED CORPORATE STRATEGY
4	ADVANCED COMPUTER ORGANIZATION	**4**	GROUNDWATER MANAGEMENT	**4**	PROFESSIONAL ETHICS AND HUMAN VALUES
5	VLSI SIGNAL PROCESSING	**5**	CYBER SECURITY	**5**	UNIVERSAL HUMAN VALUES
6	WIRELESS SENSOR NETWORKS	**6**	INTRODUCTION TO MACHINE LEARNING	**6**	ENGLISH FOR RESEARCH PAPER WRITING
7	RADAR & NAVIGATION SYSTEMS	**7**	DEEP LEARNING	**7**	DISASTER MANAGEMENT
8	WIRELESS MOBILE COMMUNICATION	**8**	ETHICAL HACKING	**8**	SANSKRIT FOR TECHNICAL KNOWLEDGE
9	CMOS RF IC DESIGN	**9**	BIG DATA TECHNOLOGIES	**9**	VALUE EDUCATION
10	IOT ARCHITECHTURES AND PROTOCOLS	**10**	E-COMMERCE	**10**	STRESS MANAGEMENT BY YOGA
11	CPLD AND FPGA ARCHITECTURES	**11**	DATA STRUCTURE AND ALGORITHMS USING JAVA	**11**	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
12	SEMICONDUCTOR DEVICE MODELLING	**12**	NATURAL LANGUAGE PROCESSING	**12**	MANAGERIAL ECONOMICS & FINANCIAL ANALYSIS
13	SYSTEM ON CHIP DESIGN	**13**	DATA ANALYTICS WITH PYTHON		
14	VLSI DESIGN FLOW	**14**	BASICS OF ARTIFICIAL INTELLIGENCE		
15	OPTICAL FIBER COMMUNICATION	**15**	INTRODUCTION TO PYTHON PROGRAMMING		
16	DIGITAL IC DESIGN	**16**	PATTERN RECOGNITION AND APPLICATIONS		

SUBJECT FOR HONOURS

POOL-1: Instrumentation and Control Systems: (any four of the following subjects which are not chosen as professional electives are to be considered for Honors Degree)

S. No.	Subject	L-T-P	Credits
1	Data Acquisition systems	3-1-0	4
2	Adaptive Control Systems	3-1-0	4
3	Bio-Medical Instrumentation	3-1-0	4
4	Digital Control Systems	3-1-0	4
5	Process Control Instrumentation	3-1-0	4
6	Transducers & sensors	3-1-0	4
7	MEMS	3-1-0	4
8	Intelligent & Smart Instrumentation	3-1-0	4
In addition to any of the four subjects, MOOC/NPTEL Courses for 04 credits (02 courses@ 2 credits each) are compulsory in the domain of Electronics and Communication Engineering			

POOL-2: Integrated circuits and Systems: (any four of the following subjects which are not chosenas professional electives are to be considered for Honors Degree)

S. No	Subject	L-T-P	Credits
1	VLSI Technology and Design	3-1-0	4
2	CMOS Analog IC Design	3-1-0	4
3	CMOS Digital IC design	3-1-0	4
4	Design for Testability	3-1-0	4
5	System on Chip	3-1-0	4
6	Programmable Logic Devices and ASIC	3-1-0	4
7	Scripting Language	3-1-0	4
8	Low Power VLSI Design	3-1-0	4
In addition to any of the four subjects, MOOC/NPTEL Courses for 04 credits (02 courses@ 2 credits each) are compulsory in the domain of Electronics and Communication Engineering			

POOL-3: Communication Engineering: (any four of the following subjects which are not chosen as aprofessional electives are to be considered for Honors Degree)

S. No	Subject	L-T-P	Credits
1	Information Theory and Coding	3-1-0	4
2	Software Defined Radio	3-1-0	4
3	Data Communications & Computer Networks	3-1-0	4
4	Telecommunication System	3-1-0	4
5	5G Communications	3-1-0	4
6	Satellite communication	3-1-0	4
7	Optical Communication	3-1-0	4
8	Audio and Video Engineering	3-1-0	4
In addition to any of the four subjects, MOOC/NPTEL Courses for 04 credits (02courses@ 2 credits each) are compulsory in the domain of Electronics and Communication Engineering			

POOL-4: Digital Signal processing (any four of the following subjects which are not chosen asprofessional electives are to be considered for Honors Degree)

S. No	Subject	L-T-P	Credits
1	Speech Signal Processing	3-1-0	4
2	Video Signal Processing	3-1-0	4
3	Adaptive Signal Processing	3-1-0	4
4	Bio- Medical Signal Processing	3-1-0	4
5	DSP Processors and Architectures	3-1-0	4
6	Wavelet Theory	3-1-0	4
7	Multirate Systems And Filter Banks	3-1-0	4
8	Mathematical methods for signal processing	3-1-0	4
In addition to any of the four subjects, MOOC/NPTEL Courses for 04 credits (02courses@ 2 credits each) are compulsory in the domain of Electronics and Communication Engineering			

GENERAL MINOR TRACKS

S. No.	Subject	L-T-P	Credits
1	Electronic Devices and Basic Circuits	3-1-0	4
2	Digital Electronics	3-1-0	4
3	Principles of communication	3-1-0	4
4	Signal Analysis	3-1-0	4
In addition to any of the four subjects, MOOC/NPTEL Courses for 04 credits (02 courses@ 2 credits each) are compulsory in the domain of Electronics and Communication Engineering			

With effect from the academic year 2022-23

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY
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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Numerical Methods and Complex Variables

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22BS3T1**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. The course is designed to equip the students with the necessary mathematical skills and techniques that are essential for an engineering course. 2. The skills derived from the course will help the student from a necessary base to develop analytic and design concepts.	On completion of the course, studentswill be able to 1. Calculate a root of algebraic and transcendental equations. 2. Compute interpolating polynomial for the given data. Explain relation between the finite difference operators. 3. Solve ordinary differential equations numerically using Euler's and RK method. 4. Verify analyticity of functions. 5. Calculate Taylor and Laurent series for functions by useing line and contour integration to evaluate integrals, Use residues to evaluate integrals.

UNIT-I : SOLUTION OF ALGEBRAIC AND TRANSCENDENTAL EQUATIONS

Introduction- Bisection Method – Method of False Position – Iteration Method – Newton-Raphson Method

UNIT-II: Interpolation

Introduction- Errors in Polynomial Interpolation – Finite differences- Forward Differences- Backward differences –Central differences – Symbolic relations and separation of symbols-Differences of a polynomial-Newton's, Gauss formulae for interpolation – Interpolation with unevenly spaced points - Lagrange"s Interpolation formula

UNIT-III: Numerical Differentiation and Integration

Integration by Trapezoidal and Simpson's rules; solution by Taylor"s series-Picard"s method of successive Approximations-Euler"s Method-Runge-Kutta Methods

UNIT-IV: Functions of a complex variable

Complex function, Real and imaginary parts of Complex function,Limit and Continuity and Derivative of a complex function, Cauchy-Reimann equations, Analytic function, entire function, singular point, conjugate function, C-R equations in polar form, Harmonic functions, Milne-Thompson method

UNIT-V: Series expansion and Complex Integration

Line integral of a Complex function, Cauchy's theorem(only statement), Cauchy's integral formula, Taylor's series, Maclaurin's series expansion, Laurent's series, Residue theorem (without proof), Calculation of residues, Residue at a pole of order m

LEARNING RESOURCES

Text Books:

1. B.S.Grewal, Higher Engineering Mathematics, 43rd Edition, Khanna Publishers

2. N.P.Bali, Engineering Mathematics, Lakshmi Publications.

References:

1. Dean G. Duffy, Advanced engineering mathematics with MATLAB, CRC Press

2. V.Ravindranath and P.Vijayalakshmi, Mathematical Methods, Himalaya Publishing House.

3. Erwin Kreyszig, Advanced Engineering Mathematics, 10th Edition, Wiley-India

4. David Kincaid, Ward Cheney, Numerical Analysis-Mathematics of Scientific Computing, 3rd Edition, Universities Press.

5. Srimanta Pal, Subodh C.Bhunia, Engineering Mathematics, Oxford University Press.

6. Dass H.K., Rajnish Verma. Er., Higher Engineering Mathematics, S. Chand Co. Pvt. Ltd, Delhi.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SWITCHING THEORY AND LOGIC DESIGN

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22BS3T2**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To provide insights of various number systems, Boolean functions and logic gates. 2. To introduce different minimization techniques. 3. To explain the design process of various combinational and sequential circuits. 4. To introduce the design of synchronous and asynchronous sequential circuits.	Upon successful completion of the course,the students will be able to 1. Convert one number system to another, analyze logic gates and Boolean theorems. 2. Analyze digital circuits using different minimization techniques. 3. Design various combinational and sequential circuits along with applications. 4. Design counters and state machines by applying the knowledge of synchronous and asynchronous sequential circuits.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2	2										3		
CO2	2	2	2	2									3		
CO3	2	2	2	2									3		
CO4	2		2		2								3		
CO5	2		2		2								3		

UNIT-I : NUMBER SYSTEMS, CODES AND BOOLEAN ALGEBRA

Number Systems, Base Conversion Methods, Complements of Numbers, 4 Bit Codes-BCD, Excess-3, 2421, 8421 codes. Even and Odd parity, Hamming code, Error detecting and Error correcting codes. Fundamentals of Boolean Algebra and Logic Gates, Boolean theorems and proofs.

UNIT-II: BOOLEAN FUNCTIONS AND MINIMIZATION

Boolean SOP and POS functions-Canonical and Standard. Realization with Universal Gates Simplification of Boolean functions using Karnaugh Map (upto 6 variables) and Quine McClusky methods.

UNIT-III: COMBINATIONAL LOGIC CIRCUITS AND DESIGN

Logic Design of Combinational circuits – Binary Adder, Subtractor, Decoders, Encoders, Multiplexers, Demultiplexers, Code Convertors, Priority Encoders, Seven–segment Displays,4-bit digital Comparators.

UNIT-IV: SEQUENTIAL LOGIC CIRCUITS AND DESIGN

RS & SR latches, clocked RS, SR, JK, T & D Flip- flops with pre-set and clear inputs. Race around problem, MS-JK-FF, Excitation tables of all Flip- Flops and conversions from one type to another. Design of Shift Registers with SIPO, SISO, PIPO and PISO modes and universal shift register. Design of Ring counters and Johnson counters.

UNIT-V: ASYNCHRONOUS AND SYNCHRONOUS SEQUENTIAL CIRCUITS

Design of Asynchronous counters (Ripple counters) for any modulus. Design of Synchronous counters using SR, JK, T and D- Flip Flops. Analysis and Design of Synchronous circuits with State Diagrams and State Reduction. Mealy to Moore conversion and vice-versa

LEARNING RESOURCES

Text Books:

1. Digital Design, Morris Mano, PHI, 3rd Edition, 2001
2. Switching and Finite Automata Theory, 2nd Edition, ZviKohavi, Tata McGraw-Hill, 1978.

References:

1. Fundamentals of Digital Circuits by A. Anand Kumar, PHI learning Pvt. Ltd
2. Fundamentals of Logic Design, Charles H Roth, Thomson Publications, 5th edition, 2009.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Electronic Devices and Circuits

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 3:2:0	SEE Marks : 70	Course Code: **22EC3T3**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To learn and understand the basic concepts of semi conductor physics and Study the physical phenomena such as conduction, transport mechanism and characteristics of different diodes. 2. To learn and understand the application of diodes as rectifiers with their operation and characteristics with and without filters are discussed. 3. Acquire knowledge about the principle of working and operation of Bipolar Junction Transistor and Field Effect Transistor and their characteristics. 4. To learn and understand the purpose of transistor biasing and its significance. 5. To analyze the Small signal equivalent circuit of BJT amplifiers and compare different configurations.	On completion of the course, students will be ableto 1. Apply the basic concepts of semiconductor physics and understand the formation of p-n junction and how it can be used in different modes of operation. 2. Able to construct the Rectifiers and filters. 3. Understand the working and characteristics of BJT and FET with the V-I characteristics in different configurations. 4. Know the need of transistor biasing, various biasing techniques for BJT and stabilization concepts with necessary expressions. 5. Perform the analysis of the small signal model of a BJT.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	1										2	
CO2	3	1	1										2	
CO3	3	1	1		1		1						2	
CO4	3	2	1		1								2	
CO5	3	2		1			1						2	

UNIT - I : PN JUNCTION CHARACTERISTICS

Review of Semiconductor physics: (Intrinsic and Extrinsic semiconductors, Conduction and Fermi level in semiconductors, Drift and Diffusion currents, Hall effect),

Junction Diode Characteristics: Open circuited p-n junction, P-N junction – open circuit, Reverse-biased, and Forward-biased PN junction; diode current equation, V-I characteristics of PN-Junction diode, Effect of temperature on PN junction diode. Diode resistance, Diode capacitance. Junction Breakdown: Avalanche and Zener breakdown.

Special Semiconductor Diodes: Characteristics of Zener Diode, Varactor Diode, Tunnel Diode, Photo Diode, and LED.

UNIT - II : RECTIFIERS AND FILTERS

Basic Rectifier setup, half wave rectifier, full wave rectifier, bridge rectifier, derivations of characteristics of rectifiers, rectifier circuits-operation, input and output waveforms, Filters: Inductor filter, Capacitor filter, π- Filter, comparison of various filter circuits. Zener diode as voltage regulator.

UNIT - III: TRANSISTOR CHARACTERISTICS

BJT: Junction transistor, transistor current components, transistor configurations, transistor as an amplifier, and characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, punch through/ Reach through effect.

FIELD EFFECT TRANSISTOR

FET: FET types, construction, operation, characteristics μ, gm, rd parameters, MOSFET-types, construction, operation, characteristics, comparison between JFETand MOSFET.

UNIT –IV: TRANSISTOR BIASING AND THERMAL STABILIZATION

Need for biasing, operating point, load line analysis, basic stability, Stability factors, (S, S', S''), BJT biasing- methods: fixed bias, collector to base bias, self-bias, Stabilization against variations in V_{BE}, I_c, and β, Bias compensation, Thermal runaway, Thermal stability.

UNIT – V: SMALL SIGNAL LOW FREQUENCY TRANSISTOR

AMPLIFIER MODEL

BJT: Two port networks and the transistor Hybrid model, Analysis of a Transistor Amplifier circuit using h- parameters, Analysis of CB, CE, and CC amplifier using exact and approximate analysis, Comparison of Transistor Amplifiers.

Learning Resources:

Text Books:

1. Electronic Devices and Circuits- J. Millman, C. Halkias, Tata Mc-Graw Hill, Second Edition.
2. Integrated Electronics- Jacob Millman, C. Halkies, C.D.Parikh, Tata Mc-Graw Hill, 2009.
3. Electronic Devices and Circuits-K. Lal Kishore, BS Publications, Fourth Edition, 2016.
4. Electronics devices & circuit theory-Robert L.Boylestad and Loui Nashelsky, Pearson / Prentice hall, tenth edition, 2009.

References:

1. Electronic Devices and Circuits-K. Satya Prasad, VGS Book Links.
2. Electronic Devices and Circuits-Salivahanan, Kumar, Vallavaraj, Tata Mc-Graw Hill, Second Edition.
3. Electronic Devices and Circuits – Bell, Oxford

With effect from the academic year 2022-23

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

CIRCUIT THEORY

SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EE4T4**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To understand the applications of network topology to electrical circuits. 2. To study the performance of R-L, R-C and R-L-C circuits with variation of one of the parameters and to understand the concept of resonance.	On completion of the course, studentswill be able to 1. Solve various electrical networks in presence of active and passive elements. 2. Understand network topology concepts. 3. Solve any magnetic circuit with various dot conventions. 4. Analyze & plot locus diagrams for R-L, L-C, R-C network with sinusoidal excitation. 5. Solve any electrical network by Network theorems.

UNIT-I : INTRODUCTION TO ELECTRICAL CIRCUITS

Network elements classification: Electric charge and current, Electric energy and potential, Resistance parameter – series and parallel combination, Inductance parameter – series and parallel combination, Capacitance parameter – series and parallel combination. Energy sources: Ideal, Non-ideal, Independent and dependent sources, Source transformation, Kirchoff's laws, Mesh analysis and Nodal analysis problem solving with resistances only including dependent sources also

Fundamentals and Network Topology: Definitions of terms associated with periodic functions: Time period, Angular velocity and frequency, RMS value, Average value, Form factor and peak factor- problem solving, Phase angle, Phasor representation, Addition and subtraction of phasors, mathematical representation of sinusoidal quantities, explanation with relevant theory, problem solving. Principal of Duality withexamples. Network Topology: Definitions of branch, node, tree, planar, non-planar graph, incidence matrix, basic tie set schedule, basic cut set schedule

UNIT-II: TRANSIENTS

First order differential equations, Definition of time constants, R-L circuit, R-C circuit with DC excitation, Evaluating initial conditions procedure, second order differential equations, homogeneous, non-homogenous, problem solving using R-

L-C elements with DC excitation and AC excitation, Response as related to s-plane rotation of roots. Solutions using Laplace transform method

UNIT-III: STEADY STATE ANALYSIS OF A.C CIRCUITS

Impedance concept, phase angle, series R-L, R-C, R-LC circuits problem solving. Complex impedance and phasor notation for R-L, R-C, R-L-C problem solving using mesh and nodal analysis, Star-Delta conversion, problem solving

UNIT-IV: RESONANCE

Introduction, Definition of Q, Series resonance, Bandwidth of series resonance, Parallel resonance, Condition for maximum impedance, current in anti resonance, Bandwidth of parallel resonance, general case-resistance present in both branches, anti resonance at all frequencies.

Network Theorems:Thevinin's, Norton's, Milliman's, Reciprocity, Compensation, Substitution, Superposition,Max Power Transfer, Tellegens- problem solving using dependent sources also

UNIT-V: TWO-PORT NETWORKS

Relationship of two port networks, Z-parameters, Y-parameters, Transmission line parameters, h-parameters, Inverse h-parameters, Inverse Transmission line parameters, Relationship between parameter sets, Parallel connection of two port networks, Cascading of two port networks, series connection of two port networks, problem solving including dependent sources also.

LEARNING RESOURCES

Text Books:

1. Engineering Circuit Analysis by William Hayt and Jack E.Kemmerley, McGraw Hill Company,6th edition

2. Network Analysis: Van Valkenburg; Prentice-Hall of India Private Ltd

References:

1. Fundamentals of Electrical Circuits by Charles K.Alexander and Mathew N.O.Sadiku, McGraw Hill Education (India)

2. Linear Circuit Analysis by De Carlo, Lin, Oxfordpublications

3. Electric Circuits– (Schaum's outlines) by MahmoodNahvi& Joseph Edminister, Adapted by KumaRao, 5th Edition – McGrawHill.

4. Electric Circuits by David A. Bell, Oxfordpublications

5. Introductory Circuit Analysis by Robert L Boylestad, PearsonPublications

6. Circuit Theory (Analysis and Synthesis) byA.Chakrabarthi,DhanpatRai&Co.

With effect from the academic year 2022-23

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

(VLSI DESIGN & TECHNOLOGY)

PRINCIPLES OF COMMUNICATION

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EV3T5**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

UNIT - I : Analog Communication

Principle of modulation, generation and detection of AM, DSBSC, SSBSC, FM signals. Quantitative analysis of continuous wave modulation, frequency division multiplexing, Introduction to transmitters and receivers, Super heterodyne receiver.

UNIT - II : Pulse Communication

Principles of Pulse modulation- generation and detection of PAM, PWMand PPM signals, quantization, Pulse code modulation (PCM), Differential pulse code modulation, Delta modulation, Time Division multiplexing.

UNIT - III : Noise in communication systems

Gaussian and white noise characteristics, Noise in AM, FM systems, Pre emphasis and De-emphasis, Threshold effect in angle modulation. Noise Considerations in PCM and DM, Optimum detection of signals in noise, Coherent receiver, matched filter -Probability of Error evaluations.

UNIT - IV : Digital communication

Baseband Pulse Transmission- Inter symbol Interference and Nyquist criterion. Pass band Digital Modulation schemes- PSK, FSK, QAM, CPM and MSK, Digital Modulation tradeoffs.

UNIT - V : Spread spectrum communications

Need for spreading a code, generation and characteristics of PN sequences. Direct Sequence Spread Spectrum and Frequency hopping spread spectrum systems and their applications. Acquisition schemes for spread spectrum receivers, Tracking of FH and DS signals.

Learning Resources:

1. Simon Haykin, “Communication Systems,” 4/e, Wiley India, 2011.
2. Sam Shanmugham.K., “Digital and Analog Communication Systems” Wiley, 2005.
3. Communication Systems (Analog and Digital) by Dr. Sanjay Sharma, 2013
4. Singh, R.P. and Sapre, S.D., “Communication Systems,” TMH, 2012.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

SWITCHING THEORY AND LOGIC DESIGN LAB

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 0:0:3	SEE Marks : 35	Course Code: **22EC3L1**
Credits : 1.5	CIE Marks : 15	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To outline the basics of Digital Electronics, Boolean algebra and be able to design the simple logic circuits and verify the functionality. 2. Design combinational and sequential logic circuits using digital ICs. 3. This laboratory course enables students to get practical experience in design, assembly and evaluation of switching theory and logic design. Students use a digital trainer kit an Xilinx simulator to test their electronic designs.	On completion of the course, studentswill be able to 1. Analyze and design basic combinational logic circuits using Digital IC's and HDL programming. 2. Implement basic sequential logic circuits using Digital IC's and HDL programming.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	2		2								3	1
CO2	2	2	2		2								3	1

List of Programs : (Minimum 10 experiment)

A.HARDWARE

1. Verification of truth tables of Logic gates Two input (i) OR (ii) AND (iii) NOR (iv) NAND (v) Exclusive OR (vi) Exclusive NOR
2. Design full adder circuit and verify its functional table.
3. Verification of functional table of 3 to 8 line Decoder/De-multiplexer using IC 74138.
4. Construct 7 Segment Display Circuit Using Decoder and 7 Segment LED and test it.

5. 4 variable logic function verification using 8 to1 multiplexer IC 74151.
6. Verification of functional tables of (i) RS and SR Latch (ii) JK Edge triggered Flip–Flop (iii) D Flip-Flop
7. Design a four bit ring counter and Johnson counter using D Flip–Flops/JK Flip Flop and verify output.
8. Design and Verify Decade Counter using IC 7490.

B. Software

9. HDL code to design 8 to 3 Encoder using Xilinx Simulator.
10. HDL Code to design binary to gray code converter using Xilinx Simulator.
11. HDL code to design Universal shift Register using Xilinx Simulator.
12. HDL Code to design Mod 8 Synchronous counter using Xilinx Simulator.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Electronics Devices and Circuits Lab

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 0:0:3	SEE Marks : 35	Course Code: **22EC3L2**
Credits : 1.5	CIE Marks : 15	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
• To develop an understanding of the characteristics of Electronic devices and circuits with Qualitative approach.	On completion of the course, students will be able to 1. Estimate the parameters from V-I Characteristics of different diodes. 2. Design various rectifiers with different filter combinations. 3. Set up bias point of a transistor. 4. Estimate the parameters from BJT and FET characteristics. 5. Compute the bandwidth of amplifier.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	2	2											2	
CO2	1	1	3											2	
CO3	1	2	3											2	
CO4	1	2	3											2	
CO5	1	2	3											2	

List of Experiments: (Minimum of Ten Experiments has to be performed)

Study experiments:

1. Identification, Specifications, Testing of R, L, C Components (Colour Codes), Bread Boards,Specifications and Testing of active devices: Diodes, BJTs, JFETs, LED.
2. Study and operation of Digital Multimeter, Function Generator, Regulated Power Supply, and CRO.

CYCLE - I Experiment:

3. PN Junction Diode Characteristics.
4. Zener diode Characteristics.
5. Half-Wave Rectifier (with and without filters)
6. Full wave rectifier (with and without filters)
7. BJT Characteristics (CE Configuration)

8. BJT Characteristics (CB Configuration)

CYCLE - II Experiments:

9. FET Characteristics (CS Configuration)
10. CRO Operation and its Measurements
11. UJT Characteristics
12. Transistor Biasing
13. BJT- CE Amplifier
14. Emitter Follower-CC Amplifier

New / Additional experiments planned

1. MOSFET as a switch in Micro wind and in Multisim tools.
2. V-I Characteristics of Light Emitting Diode.

Mini Project(s)

Designing of various basic applications using devices.

Equipment required:

1. Regulated Power supplies
2. Analog/Digital Storage Oscillo scopes
3. Analog/Digital Function Generators
4. Digital Multi-meters
5. Decade Résistance Boxes/Rheostats
6. Decade Capacitance Boxes
7. Ammeters (Analogor Digital)
8. Voltmeters (Analogor Digital)
9. Active & Passive Electronic Components

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING (VLSI DESIGN & TECHNOLOGY)

Communication Lab

SYLLABUS FOR B.TECH. IV – SEMESTER

L:T:P (Hrs./week): 0:0:3	SEE Marks : 35	Course Code: **22EV3L3**
Credits : 1.5	CIE Marks : 15	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To demonstrate analog and digital communication modulation and demodulation schemes for a given signal.	On completion of the course, students will be able to 1. Estimate the transmitted power and bandwidth of analog modulation scheme. 2. Apply concepts of multiplexing to RF signals in time domain and frequency domain. 3. Demonstrate radio signal reception using superheterodyne receiver. 4. Distinguish various line coding and source encoding schemes for digital data transmission.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3			3				2	2			3	3	
CO2	1	2	1						1	2		2	2	3	
CO3	2	1	1		2				2	2		2	2	3	
CO4	1	1							1	2			1	2	

Cycle-I: HARDWARE EXPERIMENT (Minimum 10 experiments)

1. Amplitude Modulation &Demodulation
2. DSB SC - Modulation &Demodulation
3. SSB SC - Modulation &Demodulation
4. Diode Detector
5. Pre-emphasis &De-emphasis
6. Frequency Modulation – Modulation &Demodulation
7. Verification of Sampling Theorem
8. Pulse Code Modulation
9. Pulse Amplitude Modulation & Demodulation
10. PWM, PPM –Modulation & Demodulation

11. PLL IC-565 as FM demodulator
12. Time division multiplexing.
13. Pulse code modulation.
14. Differential pulse code modulation.
15. Delta modulation.
16. Frequency shift keying.
17. Phase shift keying.
18. Differential phase shift keying.

Cycle-II: SOFTWARE EXPERIMENT (Minimum 3 experiments)

1. Amplitude Modulation &Demodulation (by using MATLAB CODING)
2. DSB SC - Modulation &Demodulation (by using MATLAB CODING)
3. Frequency Modulation – Modulation &Demodulation (by using MATLAB CODING)
4. Time division multiplexing. (by using SIMULINK)

New / Additional experiments planned:

1. Spectrum Analysis of Modulated signal using Spectrum Analyzer
2. receiver characteristics
3. Radio Receiver/TV Receiver Demo kits or Trainees

Equipment required for Laboratories:

1. RPS - 0 – 30 V
2. CRO - 0 – 20 MHz.
3. Function Generators - 0 – 1 MHz
4. RF Generators - 0 – 1000 M Hz./0 – 100 MHz.
5. Rated Voltmeters and Ammeters
6. Lab Experimental kits for Digital Communication
7. Discrete Components
8. Breadboards and Multimeters
9. Spectrum Analyzer
10. MATLAB

With effect from the academic year 2022-23

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY
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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Indian Traditional Knowledge

SYLLABUS FOR B.TECH III – SEMESTER

L:T:P (Hrs./week): 2:0:0	SEE Marks : 00	Course Code: **22EC3MC1**
Credits : 0	CIE Marks : 00	Duration of SEE : 0 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the Importance of roots of knowledge system.	On completion of the course, students will be able to 1. Understand the concept of Traditional knowledge and its importance. 2. Know the need and importance of protecting traditional knowledge. 3. Know the various enactments related to the protection of traditional knowledge. 4. Understand the concepts of Intellectual property to protect the traditional knowledge 5. Understand the traditional knowledge in different sectors.

UNIT - I : Introduction to traditional knowledge

Define traditional knowledge, nature and characteristics, scope and importance, kinds of traditional knowledge, the physical and social contexts in which traditional knowledge develop, the historical impact of social change on traditional knowledge systems. Indigenous Knowledge (IK), characteristics, traditional knowledge vis-à-vis indigenous knowledge, traditional knowledge Vs western knowledge traditional knowledge vis-à-vis formal knowledge

UNIT - II : Protection of traditional knowledge

The need for protecting traditional knowledge Significance of TK Protection, the value of TK in the global economy, Role of Government to harness TK

UNIT - III : Legal framework and Traditional Knowledge

A: The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006, Plant Varieties Protection and Farmers Rights Act, 2001 (PPVFR

Act); B: The Biological Diversity Act 2002 and Rules 2004, the protection of traditional knowledge bill, 2016. Geographical indications act 2003.

UNIT - IV : Traditional knowledge and intellectual property

Systems of traditional knowledge protection, Legal concepts for the protection of traditional knowledge, Certain non IPR mechanisms of traditional knowledge protection, Patents and traditional knowledge, Strategies to increase protection of traditional knowledge, global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT - V : Traditional knowledge in different sectors

Traditional knowledge and engineering, Traditional medicine system, TK and biotechnology, TK in agriculture, Traditional societies depend on it for their food and healthcare needs, Importance of conservation and sustainable development of environment, Management of biodiversity, Food security of the country and protection of TK

Learning Resources:

Text Books:

1. Traditional Knowledge System in India, by Amit Jha, 2009.
2. Traditional Knowledge System and Technology in India by Basanta Kumar Mohanta and Vipin Kumar Singh, Pratibha Prakashan 2012.

References:

1. Traditional Knowledge System in India by Amit Jha Atlantic publishers, 2002
2. "Knowledge Traditions and Practices of India" Kapil Kapoor, Michel Danino

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Probability and Statistics

SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22BS4T1**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To acquaint students with the fundamental concepts of probability and statistics and to develop an understanding of the role of statistics in engineering. 2. Introduce numerical techniques to solve the real world applications.	On completion of the course, studentswill be able to 1. Examine, analyze, and compare various Probability distributions for Discrete and Continuous random variable. 2. Test the hypothesis concerning mean, proportion and variance and perform ANOVA test. 3. Fit a curve to the numerical data and establish a relationship between two are more variables. 4. Evaluate clustering models to find useful patterns in unsupervised data. 5. Preparing different control charts and check whether the process is in control or not

UNIT-I : RANDOM VARIABLES AND DISTRIBUTIONS

Introduction-Random variables- Discrete and continuous Random variable-Distribution function-Expectation-. Binomial, Poisson and Geometric distributions, Uniform, Exponential and Normal distributions

UNIT-II: INTERPOLATION

Introduction - Population and samples- Sampling distribution of means (s known)-Central limit theorem- Point estimation- Maximum error of estimate - Interval estimation. Introduction –Hypothesis-Null and Alternative Hypothesis-Type I and Type II errors –Level of significance - One tail and two-tail tests-
t test- ANOVA for one-way and two-way classified data

UNIT-III: CURVE FITTING AND CORRELATION

Introduction - Fitting a straight line –Second degree curve-exponential curve-power curve by method of least squares-Goodness of fit. Correlation & Covariance- Linear Regression and Multiple Regression, Generalized linear models- Poisson regression, Logistic Regression, Survival Analysis-Splines

UNIT-IV: ADVANCED STATISTICS

Classification-K-Nearest Neighbors (K-NN), Support Vector Machines (SVM), Naïve Bayes, Decision Trees, Random Forests, **Clustering:** K-Means Clustering, Hierarchical Clustering**.** Dimentionality reduction-Principal Component Analysis (PCA), Linear Discriminant Analysis (LDA)

UNIT-V: STATISTICAL QUALITY CONTROL METHODS

Introduction - Methods for preparing control charts – Problems using x-bar, R charts, Sigma Chart and attribute charts.

LEARNING RESOURCES

Text Books:

1. **Jay l.devore,** Probability and Statistics for Engineering and the Sciences.8th edition, engage.

2. **Richards A Johnson, Irvin Miller and Johnson E Freund**. Probability and Statistics for Engineering, 9th Edition,PHI

References:

1. **Shron L.Myers, Keying Ye, Ronald E Walpole,** Probability and Statistics Engineers and the Scientists,8th Edition, Pearson 2007.

2. **William Menden Hall, Robert J. Bever and Barbara Bever**, Introduction to probability and statistics, Cengage learning.2009

3. **Sheldon, M. Rosss**, Introduction to probability and statistics Engineers and the Scientists, 4th edition, Academic Foundation,2011

4. **Johannes Ledolter and Robert V.Hogg**, Applied statistics for Engineers and Physical Scientists, 3rd Edition,Pearson,2010

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CMOS ANALOG IC DESIGN

SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **23EVT4B**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. **To develop a strong foundation in MOS devices and modeling**, including understanding MOS transistor operation, layout fundamentals, and various MOS models such as large-signal, small-signal, and sub-threshold models. 2. **To understand the design and analysis of analog CMOS sub-circuits**, including MOS switches, diodes, active resistors, current sources, current mirrors, and voltage/current reference circuits such as bandgap references. 3. **To enable students to analyze and design CMOS amplifier circuits**, including inverters, differential pairs, cascode amplifiers, current and output amplifiers, and high-gain amplifier architectures. 4. **To provide a comprehensive understanding of CMOS operational amplifier design**, focusing on two-stage and cascode op-amps, frequency compensation techniques, PSRR improvement, and practical measurement/characterization methods. 5. **To introduce comparator circuits and their performance parameters**, covering two-stage and open-loop comparators, advanced comparator topologies, performance enhancement techniques, and discrete-time comparators.	1. Understand MOS device operation, modeling, and small-signal/large-signal behavior.. 2. Analyze CMOS sub-circuits such as current mirrors, switches, and biasing networks. 3. Design and evaluate CMOS amplifiers including differential, cascode, and multistage amplifiers. 4. Design CMOS operational amplifiers and apply compensation techniques for stability improvement. 5. Analyze and design CMOS comparators, including open-loop and dynamic comparators.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1							1	3	3
CO2	3	2	3	2	2							1	3	2
CO3	3	3	3	2	2							1	3	2
CO4	3	3	3	3	2						1	2	3	3
CO5	3	3	2	2	2							1	2	2

Unit – I MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

Unit-II Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

Unit-III CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

Unit-IV CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

Unit-V Comparators

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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Digital Signal Processing

SYLLABUS FOR B. TECH IV - SEMESTER

L: T: P (Hrs./week): 3:0:0	SEE Marks: 70	Course Code: **22ET4T3**
Credits: 3	CIE Marks: 30	Duration of SEE: 3 Hours

COURSE OBJECTIVES
1. This course introduces discrete time signals, systems and operations performed on them.
2. It introduces Discrete Time Fourier Transform, Discrete Fourier Transform and Z Transform meant for spectral analysis of discrete time signals and systems.
3. It also introduces Fast Fourier Transform that is an efficient way of implementing DFT.
4. It provides the basic knowledge about the design of both IIR and FIR filters.

COURSE OUTCOMES: On completion of the course, students will be able to	
CO 1	Understand the basics of discrete time signal processing techniques, classify and perform operations on discrete-time signals.
CO 2	Analyze and apply Z-Transform for causal, anti-causal and non-causal sequences including ROC and properties.
CO 3	Compute and analyze the Discrete Fourier Transform (DFT), relate DFT with DTFT and apply DTFT, DFT, FFT and Z-Transform techniques to solve and realize discrete systems
CO 4	Design of IIR digital filters using different filtering techniques, and apply analog frequency transformations for obtaining various filter types.
CO 5	Design of FIR filters using Fourier Series method and different windowing techniques.

CO-PO/PSO Mapping:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	**3**	**2**										**1**		
CO 2	**3**	**3**		**2**	**3**							**1**	**2**	**2**
CO 3	**3**	**3**	**2**	**3**	**3**							**1**	**2**	**2**
CO 4	**3**	**3**	**3**	**3**	**3**							**1**	**2**	**2**
CO 5	**3**	**3**	**3**	**2**	**3**							**1**	**2**	**2**

UNIT-I:

Digital Signal Processing System (DSP) - Block diagram, Advantages, Limitations and Applications of DSP system. Discrete Time Signals: Discrete time signals - Impulse, Unit Step, Unit Ramp, Rectangular, Exponential signals, Representation of discrete time signals, Operations on signals – Time shifting, Time scaling, Time reversal, Amplitude scaling, Properties of signals -Even/Odd signals, Causal/Non-Causal signals, Bounded/Unbounded signals, Periodic/Aperiodic signals.

Discrete Time Systems: Properties of discrete time systems- Linear and Nonlinear, Shift Invariant and Variant, Causal and Non-Causal, Stable and Unstable, Static and Dynamic, IIR and FIR systems. Analysis of LTI Systems through LCCDE – Natural Response, Forced Response, Response of Linear shift invariant systems-Linear Convolution Discrete Time Fourier Transform: DTFT of a sequence and system, Frequency response, Magnitude response and Phase response. Properties of DTFT- Linearity, Periodicity, Time shifting, Frequency shifting, Time reversal, Conjugate and Parseval's theorem.

UNIT-II: Z-Transform

Z-Transform of Causal, Anti-Causal and Non-Causal sequence. Region of Convergence and Properties, Properties of Z-Transform - Linearity, Time shifting, Time reversal, Multiplication by exponential sequence, Scaling in Z-domain, Conjugate, Differentiation in Z-domain, Time Convolution, Initial Value and Final Value Theorem, Inverse Z-Transform through Long Division, Partial Fractions and Residue Methods, Analysis of LTI system using z-transforms – system function, causality, stability , solution of difference equation, impulse response and step response .Realization of Discrete Systems: Direct Form-I, Direct Form-II or Canonic Form, Cascade Form and Parallel Form for IIR and FIR systems.

UNIT – III:

Discrete Fourier Transform: Frequency sampling - DFT, Computation of DFT, Computation of IDFT, Relation between DTFT and DFT, Properties of Twiddle factor, Properties of DFT- Linearity, Periodicity, Time shifting, Frequency shifting, Time reversal, differentiation in frequency domain, Conjugate, Parseval's theorem, Circular convolution, Additional DFT properties, Linear Convolution through Circular Convolution, Circular Convolution through DFT and IDFT, Linear Convolution through DFT and IDFT.

Fast Fourier Transform: Need for FFT, Radix-2 Decimation in Time FFT Algorithm, Radix-2 Decimation in Frequency FFT Algorithm, Comparison between DIT and DIF Algorithms, Inverse FFT.

UNIT – IV: IIR Filters

Design of IIR digital filters - Impulse Invariant Transformation, Bilinear Transformation. Specifications of Low Pass Filter, Analog Butterworth Filter, Design of Low Pass Digital Butterworth Filter, Analog Chebyshev Filter, Design of Low Pass Digital Chebyshev Filter, Analog Frequency Transformations.

UNIT – V: FIR Filters

Comparison between FIR and IIR Filters, Characteristics of FIR filters with linear Phase, Frequency Response Linear Phase FIR filters, Design of FIR filters - Fourier series method, Windowing Techniques-Rectangular Window, Hanning Window, Hamming Window, Kaiser Window.

LEARNING RESOURCES:

TEXT BOOK (S):

1. John G. Proakis, Dimitris G. Manolakis-"Digital Signal Processing, Principles, Algorithms & Applications", Pearson education, 4th edition, 2008
2. Alan V Openheim, Ronald W. Schafer- "Digital Signal Processing", PHI learning, 1stedition, 2010.

REFERENCE (S):

1. P. Ramesh Babu, "Digital Signal Processing", Scitech Publications, 4th edition, 2012 Pvt Ltd.
2. A. Nagoor Kani, "Digital Signal Processing", RBA Publications,1st edition, 2005.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING (VLSI DESIGN & TECHNOLOGY)**

COMPUTER ARCHITECTURE

SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EV4T4**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

UNIT - I: DATA REPRESENTATION AND COMPUTER ARITHMETIC

Fixed point representation of numbers, digital arithmetic algorithms for Addition, Subtraction, ripple carry adder, carry look-ahead adder, Multiplication using Booth's algorithm and Division using restoring and non restoring algorithms.

Basic Structure Of Computers: Functional unit, Basic Operational concepts, Bus structures, System Software, Performance, The history of computer development.

UNIT-II: ADDRESSING MODES

Addressing Modes, Basic Input/output Operations, The role of Stacks and Queues in computer programming equation. Component of Instructions: Logic Instructions, shift and Rotate Instructions.

Type of Instructions: Arithmetic and Logic Instructions, Branch Instructions, Addressing Modes, Input/output Operation

UNIT-III: INPUT / OUTPUT ORGANIZATION

INPUT/OUTPUT ORGANIZATION: Accessing I/O Devices, Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access,

Buses: Synchronous Bus, Asynchronous Bus, Interface Circuits, Standard I/O Interface: Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB)

UNIT–IV: MEMORY SYSTEMS

The MEMORY SYSTEMS: Basic memory circuits, Memory System Consideration, Read Only Memory: ROM, PROM, EPROM, EEPROM, Flash Memory, Cache Memories: Mapping Functions, INTERLEAVING

Secondary Storage: Magnetic Hard Disks, Optical Disks,

UNIT-V: PROCESSING UNIT

Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control

Pipelining: Basic Concepts, Data Hazards, Instruction Hazards, Influence on Instruction Sets, Data Path and Control Considerations, Super Scalar Operation, UltraSPARC 2 Example, Performance Consideration

Large Computer Systems: Forms of Parallel Processing, Array Processors, the Structure of General Purpose Multiprocessors, Interconnection Networks.

Learning Resources:

TEXT BOOKS:

1. Computer Organization, Carl Hamacher, ZvonksVranesic, SafeaZaky, 5thEdition, McGraw-Hill, 2011.
2. Computer Architecture and Organization, John P. Hayes 3rdEdition, McGraw-Hill, 2002.

REFERENCE:

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson /PHI.
2. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition PHI/Pearson, 2012.
3. Fundamentals or Computer Organization and Design, – Sivaraama Dandamudi Springer Int.Edition, 2003.
4. "Computer Organization and Design: The Hardware/Software Interface" by DavidA. Patterson and John L.Hennessy, 1998.

Course Outcomes:

CO1 Identify functional units, bus structure and addressing modes
CO2 Illustrate addressing modes
CO3 Interface I/O devices with memory hierarchy.
CO4 Design Arithmetic Logic Unit. Identify memory hierarchy and performance
CO5 Design the pipelining and micro-programmed control units.

II Year - II Semester **L T P C**
3 003

DIGITAL SYTEM DESIGN THROUGH VERILOG (22EV4T5)

PROFESSIONAL ELECTIVE-II

Lecture – Tutorial:	3-0 Hours	**Internal Marks:**	30
Credits:	3	**External Marks:**	70

Prerequisites: Digital Logic Design, Digital IC Applications.

Course Objectives:

- To learn advanced digital design concepts.
- To design digital sub-systems using Verilog HDL.
- To learn Memory, CPLDs, FPGAs and ASICs.
- To Design and implementation of combinational and sequential digital logic circuits.

Course Outcomes:

Upon successful completion of the course, the student will be able to:

CO1	Model complex digital systems at several levels of abstractions, behavioral, structural, simulation, synthesisand rapid system prototyping.
CO2	Have basic understanding of Memory, CPLDs, FPGAs and ASICs.
CO3	Design digital circuits and subsystems using Verilog HDL.
CO4	Analyze and design basic digital circuits with Sequential circuits using Verilog HDL.
CO5	Apply various Digital ICs in performance evaluation for the synthesis process.

Course Content(Syllabus)

UNIT-I

Verilog HDL-Basics: Introduction, Overview of Digital Design with Verilog HDL,HierarchicalModeling Concepts, Basic Concepts, Modules and Ports, Gate Level Modeling, Dataflow Modeling**Verilog HDL-Programming:**BehavioralModeling, Tasks and Functions, Useful Modeling Techniques, Timing and Delays, User Defined Primitives, Logic Synthesis with Verilog HDL, Testbenches for verification of HDL models.

UNIT-II

Combinational Logic Design-I: Introduction, Combinational-Circuit Analysis, Combinational-Circuit Synthesis, Programmed Minimization Methods, Timing Hazards, Circuit Timing, Decoders, Encoders, Three-State Devices.Verilog Progamming for above Models

UNIT-III

Combinational Logic Design-II: Multiplexers, Exclusive-OR Gates and Parity Circuits, Comparators, Adders, Subtractors, ALUs, Combinational Multipliers.Design considerations of the above combinational logic circuits.Verilog Progamming for above Models

UNIT-IV
.**Sequential Logic Design:**Bistable Elements, Latches and Flip-Flops, Counters, Shift Registers, Clocked Synchronous State-Machine Analysis and Design, Designing State Machines Using State Diagrams.Verilog Progamming for above Models
UNIT-V
Memory and CPLDs: Read-Only Memory, Read/Write Memory, Static RAM, Dynamic RAM, Complex Programmable Logic Devices. **FPGAs and ASICs:** Field-Programmable Gate Arrays, Types of ASICs, ASIC Design flow, Economicsof ASICs.
TEXT BOOKS:
1. John F. Wakerly, *"Digital Design: Principles and Practices"*, 4th edition, Pearson, 2008 2. Samir Palnitkar, *"Verilog HDL: A Guide to Digital Design and Synthesis"*, 2nd edition,Pearson, 2003 3. Enoch O. Hwang, *"Digital Logic and Microprocessor Design with VHDL"*, 1st edition,Nelson Engineering, 2007.
REFERENCE BOOKS:
1.Michael John Sebastian Smith, *"Application-Specific Integrated Circuits"*, 1st edition,Pearson, 2002 2. Charles H. Roth, *"Fundamentals of Logic Design"*, 5th edition, Cengage Learning, 2004 3. Randy H. Katz, Gaetano Borriello, *"Contemporary Logic Design"*, 2nd edition, PHILearning, 2009

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING
(VLSI DESIGN & TECHNOLOGY)
CMOS ANALOG IC DESIGN LAB
SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 1:0:2	SEE Marks : 50	Course Code: **22EV4L1**
Credits : 1.5	CIE Marks : 00	Duration of SEE : 3 Hours

COURSE OUTCOMES: On completion of the course, students will be able to

CO1	1. Learn frequency and noise performance of amplifiers.
CO2	2. Provide hands on design experience with professional design platforms.
CO3	3. Measure difference between different toolbox.

LIST OF EXPERIMENTS: (Minimum 10 experiments)

- **Using S-Edit toolbox:**

1. Design a CMOS inverter and analyze its characteristics.
2. Design a Common source amplifier and analyze its performance.
3. Design a Common drain amplifier and analyze its performance.
4. Design a Common gate amplifier and analyze its performance.
5. Design a differential amplifier with resistive load using transistors.
6. Design three stage and five stage ring oscillator circuit and compare its frequencies.

Using L-Edit toolbox:

7. Design a CMOS inverter and analyze its characteristics.
8. Design a Common source amplifier and analyze its performance.
9. Design a Common drain amplifier and analyze its performance.
10. Design a Common gate amplifier and analyze its performance.
11. Design a differential amplifier with resistive load using transistors.
12. Design three stage and five stage ring oscillator circuit and compare its frequencies.

Requirements:

1. Cadence/Synopsis/ Mentor Graphics/Tanner/equivalent EDA Tools.

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Digital Signal Processing Lab

SYLLABUS FOR B. TECH IV - SEMESTER

L: T: P (Hrs./week): 0:0:3	SEE Marks: 35	Course Code: **22EV4L2**
Credits: 1.5	CIE Marks: 15	Duration of SEE: 3 Hours

List of Experiments:

1. Generation of discrete time Signals
2. Linear Convolutions between two given Signals.
3. Circular Convolutions between two given Signals.
4. Autocorrelation for the given sequence and Cross Correlation between two given signals.
5. Computation of N-point DFT
6. Computation of N-point IDFT
7. Linear and Circular Convolution using DFT
8. Linear and Circular Convolution using IDFT
9. Power Spectral Density for sinusoidal signal
10. Design of Digital IIR Butterworth filter using Bi-linear Transformation
11. Design of Digital IIR Chebyshev filter using Bi-linear Transformation
12. Design of Digital FIR Chebyshev filters using Windowing technique

Equipment Required:

1. PC
2. MATLAB Software

DIGITAL DESIGN THROUGH VERILOG LAB (22EV4L3)

Prerequisites:
Switching Theory and Logic Designing , C Language and Pulse & Digital Circuits Laboratory

Course Objectives:
The course should enable the students to
1. Introduce the basic HDL languages and their importance in digital design.
2. VERILOG fundamentals were discussed to modelling the digital system design blocks.
3. Model digital systems at several levels of abstractions, dataflow, behavioural, structural & mixed signalling modelling.
4. Analyze and design basic digital circuits with combinatorial and sequential logic circuits using VERILOG
5. VERILOG compilers, simulators and synthesis tools are described, which are used to verify digital systems in a technology-independent fashion.

Course Outcomes:	
Upon successful completion of the course the student will be able to	
CO1	Develop a VERILOG source code.
CO2	Perform simulation using relevant simulators.
CO3	Analysis of the obtained simulation results using necessary synthesizers.
CO4	Verify the logic with the necessary hardware.

List of Experiments :(Minimum of Ten Experiments has to be performed)

Note: The students are required to develop VERILOG source code, perform simulation using a relevant simulator, and analyze the obtained simulation results using a necessary synthesizer. All the experiments are required to verify and implement the logical operations on the latest FPGA Hardware in the Laboratory.

1. Realization of logic gates using three models.
2. Design of full adder and develop VERILOG code using three models.
3. Design 3 to 8 decoders and develop VERILOG code.
4. Design 8 to 3 encoder and develop VERILOG code.
5. Design 8 x 1 multiplexer and develop VERILOG code.
6. Design 4- Bit magnitude comparator and develop VERILOG code.

7. Design 4-Bit binary to grey code converter and develop VERILOG code.

8. Design D-Flip-Flop and develop VERILOG code.

9. Design decade counter and develop VERILOG code.

10. Design universal shift registers and develop VERILOG code.

11. Design an 8-bit serial in-parallel out and parallel in-serial out shift register and develop VERILOG L code.

12. Design ALU and develop VERILOG code.

Equipment/Software required:

1. Xilinx Vivado software / Equivalent Industry Standard Software.

2. Xilinx Hardware / Equivalent hardware.

3. Personal computer system with necessary software to run the programs and implement.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Introduction to MATLAB Programming & PCB DESIGN

SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 1:0:2	SEE Marks : 50	Course Code: **22EC4S1**
Credits : 2	CIE Marks : 00	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. Introduce the MATLAB software environment. 2. The students should be able to carry out any PCB design necessary for their graduation projects. 3. Students analyze single-sided and double-sided printed circuit board design, emphasizing the drawings, standards, and the processes required to layout printed circuit board and manufacturing documentation	On completion of the course, studentswill be able to 1. Use MATLAB effectively to analyze and visualize data. 2. Electrical, communication, computer mechatronic, energy and industrial engineering students who want to include the PCB Design experience as part of their skill set. 3. Start a career in electronics engineering. 4. create schematics from blue-prints, they will also be able to perform simple simulations

UNIT - I: MATLAB INTRODUCTION

Basics of MATLAB, MATLAB environment, MATLAB data types, MATLAB operators, MATLAB control statements, Basic command, Basic programming with simple examples

UNIT-II: PCB Design Introduction

Introduction to PCB designing concepts Introduction & Brief History, What is PCB, Difference between PWB and PCB, Types of PCBs: Single Sided (Single Layer), Multi-Layer (Double Layer), PCB Materials Introduction to Electronic design Automation (EDA), Brief History of EDA, Latest Trends in Market, How it helps and Why it requires , Different EDA tools

UNIT-III: COMPONENTS OF PCB DESIGN

Component introduction and their categories, Types of Components, Active Components, Diodeo Transistor, MOSFET , LED, SCR, Integrated Circuits (ICs), Passive Components, Resistoro Capacitor, Inductoro Transformer, Speaker/Buzzer Component, Package Types, Through Hole Packages, Axial lead o Radial Lead, Single Inline, Package(SIP), Dual Inline Package(DIP), Transistor Outline(TO), Pin Grid Array(PGA), Through Hole Packages, Metal Electrode Face(MELF), Leadless Chip Carrier(LCC), Small Outline Integrated Circuit(SOIC), Quad Flat Pack(QPF) and Thin QFP (TQFP),

Ball Grid Array(BGA), Plastic Leaded Chip Carrier(PLCC)

UNIT–IV: MATLAB PROGRAMMING PRCTICE

1. Creating matrices and arrays
2. Image import and export
3. Using scripts and functions
4. Data import and export
5. Using the graphical features

UNIT-V: PROJECT WORK ON PCB

Project work, Making the schematic of Academic and Industrial projects, PCB, Designing of these projects, Soldering and De-soldering of components as per Design, Testing and Troubleshooting Methods

Learning Resources:

1. MATLAB for Beginners: A Gentle Approach by Peter I. Kattan, Revised edition

2. Printed Circuit Boards by Khandpur

3. PCB Design : Printed Circuit Board by Michael Dsouza

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Microprocessors and Microcontrollers

SYLLABUS FOR B.Tech V SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22ET5T1**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To familiarize the students on 8086µp and 8051µc architecture. 2. To understand operation of maximum mode and minimum mode. 3. To understand the advanced micro processors features. 4. To understand the Assembly language programming with 8051. 5. To identify different advanced microcontrollers.	On completion of the course, students will be able to 1. Summarize architectural features of 8086µp. 2. Interface and program 8086µp withmemory, PPI, timer and DMA. 3. Apply the knowledge of Architectural features of 8051 µc to program 8051µc. 4. Interface and program on chip peripherals of 8051µc. 5. Interface off chip peripherals with 8051µc and design a system around 8051µc based system

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2										2		
CO2	2	2	1										1		
CO3	2	2	1	1	1								1		
CO4	3	2	1												
CO5	1	1	1	1	1								2		

UNIT - I: 8086 ARCHITECTURE

8086 PIN diagrams(Minimum mode ,Maximum mode), 8086architecture, Register set, Addressing Modes, Basic Instructions set, Assembler Directives, Memory Organization, Interrupt structure of 8086

UNIT-II: :MINIMUM AND MAXIMUM MODE OPERATIONS

Minimum and Maximum mode: operations of 8086, Timing Diagrams, General bus operation (Read,Write cycles).

Assembly language programs: Involving arithmetic expressions, logical, sorting Operations,evaluation of prostring manipulation

UNIT - III: 8086 INTERFACING AND ADVANCED MICROPROCESSORS

Memory interfacing: RAM, EPROM IC Chips I/O interfacing: 8255 PPI, 8257 DMA interface Interfacing programmable interval timers – 8253/8254

ADVANCED MICROPROCESSORS:

Introduction to Advanced Micro Processors, 80386 Architecture and Features,80386 (Real and Protected Modes) and Features, 80386(Segmentation & Paging Techniques), RISC & SISC features, Pentium processor Architecture

UNIT - IV: 8051 MICROCONTROLLER

Architecture of 8051, Pin configuration, Memory organization(ROM & RAM), Register set of 8051 , Interrupts of 8051.

Assembly language Programming with 8051: Instruction set, Datatransfer, Arithmetic, logical and Branching instructions, Addressing modes

UNIT-V:ADVANCED MICROCONTROLLERS

Block diagram of basic PIC micro controller, registers I/O ports, Addressing modes of PIC Microcontroller ARM Core Architecture,

Programming in C for PIC: Data types, I/O programming, logical operations, data conversion(BCD toASCII, ASCII to BCD)

Learning Resources:

1. Ray A.K. and Bhurchandi K.M.- "Advanced microprocessor and peripherals", 2nd edition, TMH, 2000
2. Kamal Raj- "Microcontrollers Architecture, programming, interfacing and system Design", Pearson Education,2005.
3. Gaonkar Ramesh S.- "Microprocessor Architecture, Programming, and Applications With the 8085", Prentice HallPTR, 2002
4. Mazidi Ali Muhammad- "The 8051 Micro Controller and Embedded Systems Programming using Assembly and C", second edition , Pearson Education,2007
5. Mazidi Ali Muhammad –"PIC microcontroller and Embedded Systems, Using assebly and c for PIC18"

References

1. Hall Douglas V.- "Microprocessors Interfacing", 2nd edition, 2007.
2. Triebel Walter A. and Singh Avtar- "The 8088 and 8086 Microprocessors", PHI, 4th Edition, 2003.
3. Liu and Gibson GA- "Micro-computer system 8066/8088 family Architecture, programming and Design", PHI,2nd Edition
4. Ghoshal Subrata-"Microcontroller-Internals,Instructions,Programming and Interfacing", Pearson,2010

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

DESIGN FOR TESTABILITY

Course Code: 22EV5T2

UNIT - I Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing.Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation: Compiled-Code, Event-Driven, Algorithms for Fault Simulation: Serial, Parallel, Deductive and Concurrent Fault Simulation, ATPG.

UNIT - III Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Design

SYLLABUS FOR B. TECH V SEMESTER

L: T:P (Hrs./week): 3:0:0	SEE Marks: 70	Course Code: **22EC5T3**
Credits: 3	CIE Marks: 30	Duration of SEE: 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To understand the MOS fabrication technologies, electrical properties and develop layout of MOS circuits, subsystem, Learn the VHDL coding	On completion of the course, students will be able to 1 Acquire fundamental knowledge on MOSFET characteristics and its parameters 2 Understand basic electrical properties of MOS devices. 3 Apply the design rules and analyze the impact of scaling on MOS circuits 4 Comprehend the need of hardware description language and its features 5 Design various applications using FPGA.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	2		1								2	
CO2	2	2	1										2	
CO3	1	3		3									2	
CO4	1	3	3									2	2	
CO5	2	2		2	1							2	2	

UNIT-I : MOS TRANSISTOR

Introduction to MOS Transistor Theory: NMOS, PMOS Enhancement Transistor, MOSFET as a Switch, Threshold voltage, Body effect. MOS Device Design Equations, Basic DC equations, Short Channel Effects and Device Models – Scaling Theory, Threshold Voltage Variation, Mobility Degradation with Vertical Field, Velocity Saturation, Hot Carrier Effects, Output Impedance Variation with Drain-Source Voltage, MOS Device Models

UNIT-II: BASIC ELECTRICAL PROPERTIES AND CIRCUIT CONCEPTS

MOS device design equations: drain current-voltage, threshold voltage, and transconductance. NMOS Inverter and Transfer characteristics, pull up and pull-down ratios of NMOS, alternative forms of pull up, CMOS Inverter and transfer

characteristics, Latch-up in CMOS circuits.

UNIT-III: MOS and BICMOS Circuit Design Processes and scaling

VLSI circuit design process, MOS layers, Stick and layout representations of layers Lambda and Micron based Design rules, Stick and Layout diagrams. Scaling models and scaling factors, scaling factors for device parameters, limitations of scaling.

UNIT-IV: INTRODUCTION TO VHDL

Introduction to VLSI design cycle, Computer-aided design tools for digital systems, Hardware description language: VHDL, features, Data objects, Classes and data types, Operators, Subprograms, Over loading.

UNIT-V: FPGA & ADVANCED TECHNOLOGIES

FPGA DESIGN: FPGA design flow, Basic FPGA architecture, FPGA Technologies, Introduction to FPGA Families.

INTRODUCTION TO ADVANCED TECHNOLOGIES: Giga-scale dilemma, High–k, Metal Gate Technology, Fin-FET, TFET.

LEARNING RESOURCES

Text Books:

1. Essentials of VLSI Circuits and Systems-Kamran Eshraghian, Douglas and A. Pucknell and Sholeh Eshraghian - Prentice Hall India, Private Limited, 2005 Edition.
2. Weste Neil H. E. and Eshraghian K.- “Principle of CMOS VLSI Design: A Systems Perspective” Addison Wesley, 2000.
3. Prasad K.V.K.K. Dr., Shyamala K.- “VLSI Design–Black Book”, Kogent Learning Solutions Inc.,2012
4. Perry D. L. - “VHDL: Programming by Example”, Tata McGraw-Hill, 2002.

References:

1. Brown S. and Vranesic Z.- “Fundamentals of Digital Logic with VHDL Design” McGraw-Hill Education, 2008.
2. Kang S. M., Leblebici Y.- ”CMOS digital integrated circuits: Analysis & design”, Tata McGraw-Hill, 3rd Edition, 2003.
3. Bhasker J.- “A VHDL Primmer”, Prentice Hall PTR, 1999
4. Fin-Fets and other multi-gate transistors, Colinge JP, Editor NewYork, Springer, 2008.

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (ECA & EVT)						
		Regulation : AR-22						
Subject Code	**20ET5T4F**	Hours / Week			Credit	Maximum Marks		
Subject	**RADAR & NAVIGATION SYSTEMS**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**V B Tech I Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge in Engineering							
Objectives	To familiarize with the basic principles of RADAR and operation of different types of Radars							
	To introduce different RADAR performance factors.							
	To introduce the different radar systems							
Outcomes	**At the end of this course the student can able to:**							
	Understand the basic working principle of RADAR							
	Design different radar							
	Understand the need and functioning of CW, FM-CW and MTI radars							
	Known various Tracking methods.							
	Derive the matched filter response characteristics for radar receivers.							
	Design application related antenna in accordance with Radar Receiver.							

UNIT – I: Introduction to Basic Types of RADAR

Nature of Radar, Maximum Unambiguous Range, Radar Waveforms, Simple form of Radar equation, Radar Block diagram and Operation, Radar frequencies and Applications, Radar Equation, Minimum Detectable signal

CW AND FM-CW RADAR: Doppler Effect, CW Radar-Block Diagram, Isolation between Transmitter and Receiver; Non-zero IF Receiver, Receiver Bandwidth Requirements, FM-CW Radar, Range and Doppler Measurement, Block Diagram and Characteristics(Approaching/Receding Targets),FM-CW altimeter, Measurement Errors, Multiple Frequency CW Radar

UNIT – II: MTI AND Pulse Doppler Radar

Principle, Block diagram of MTI Radar, Delay Line Cancellers-Filter characteristics, Blind Speeds, Double Cancellation, Staggered PRFs; Range Gated Doppler Filters, MTI Radar Parameters, Limitations to MTI performance, Non-coherent MTI,MTI versus Doppler Radar

UNIT – III: TRACKING RADAR

Tracking with radar, Sequential lobbing,Conical Scan,Mono-pulse Tracking Radar-Amplitude Comparison(one-and Two- Coordinates),Phase Comparison, Target Reflection Characteristics and Angular Accuracy, Tracking in Range, Acquisition and Scanning Patterns

UNIT – IV: DETECTION THEORY WITH RADAR RECEIVER

DETECTION THEORY: Receiver noise and signal to noise ratio, Integration of Radar Pulses, PRF and Range Ambiguities, System Losses, Matched Filter Receiver-Response Characteristics and Derivation, Correlation Function and Cross Correlation Receiver, Efficiency of Non-Matched Filter, Matched Filter with Non-white Noise

RADAR RECIEVERS: Noise Figure and Noise Temperature, Different types of radar displays, Duplexers-Branch type and Balanced Type, Circulators as Duplexers, Introduction to Phased Array Antennas-Basic Concepts, Radiation pattern, Beam Steering and Beam Width Changes, Series versus Parallel Feeds, Applications, Advantages and Disadvantages

UNIT – V: NAVIGATION SYSTEMS

Fundamentals of Navigation: Defination, Importance, Historical overview of Navigation, Types of Navigation, Navigation Principles

Navigation Systems: GNSS Navigation Systems, Regional Navigation Satellite Systems, Other Navigation Systems

Navigation Applications: Air Navigation, Marine Navigation, Land Navigation

Navigation Errors & Mitigation: GNSS Errors, Error Correction Methods

LEARNING RESOURCES

Text Books:

1. Merrill I. Skolnik- "Introduction to Radar Systems", TMH Special Indian Edition, 2ndEd., 2007
2. Peebles Jr., P.Z.- "Radar Principles", Wiley, New York, 1998
3. G S RAO, Global Navigation Satellite Systems, McGraw-Hill,New Delhi, 2010.

References:

1. Richards Mark A., Scheer James A., Holm William A.- "Principles of Modern Radar: Basic Principles", Yesdee, 2013.
2. Edde Byron- "Radar: Principles, Technology & Applications", Pearson Education, 2004.
3. Skolnik Merrill I.- "Radar Handbook", 3rd Ed., McGraw Hill Education, 2008
4. Rajat Acharya, Understanding Satellite Navigation, Academic Press, 2014.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATIONS ENGINEERING**

Pulse and digital circuits

SYLLABUS FOR B.TECH V SEMESTER(AR 22)

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC5T1**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To explain the complete response of R-C transient circuits. 2. To explain switching characteristics of Diode, transistors, design of Bistable multivibrator. 3. To understand the functioning of different types of time-base Generators.	On completion of the course, students will be able to 1. Understand the applications of diode as integrator, differentiator, Utilize the non-sinusoidal signals in many experimental research areas. 2. Understand the applications of diode and transistors in non-linear wave shaping circuits. 3. Learn various switching devices such as diode, transistor and Study different types of Logic families. 4. Apply the fundamental concepts of wave shaping for various signal generating circuits Multivibrators. 5. Analyze different time base generators.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	2	3									3	2	3
CO2	3	2	2	3									3	2	3
CO3	2	3		2									2	3	2
CO4	2	3		2									2	2	2
CO5	2	3	3	2									3	3	2

UNIT-I : LINEAR WAVESHAPING

High pass, low pass RC circuits, their response for sinusoidal, step, pulse, square, ramp and exponential inputs. RC network as differentiator and integrator, double differentiator Attenuators, its applications in CRO probe.

UNIT-II: NON-LINEAR WAVE SHAPING

Diode clippers, Transistor clippers, clipping at two independent levels, Transfer characteristics of clippers, Emitter coupled clipper; Clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem, Transfer characteristics of clampers.

UNIT-III: SWITCHING CHARACTERISTICS OF DEVICES

Piecewise linear diode characteristics, Diode as a switch, Design and analysis of Transistor as aswitch.

LOGIC FAMILIES: Diode Logic, Transistor Logic, Diode-Transistor Logic, Transistor-Transistor Logic, Emitter Coupled Logic, CMOS Logic, Comparison of Logic Families.

UNIT-IV: MULTIVIBRATORS

Bistable Multivibrator: Analysis And Design of Fixed Bias, Self-Bias Bistable MultiVibrator, Collector Catching Diodes, Commutating Capacitors, Triggering of Binary Circuits.

Monostable Multivibrator: Analysis and Design of Collector Coupled Monostable Multivibrator, Triggering of Monostable Multivibrator, Applications of Monostable Multivibrator.

Astable Multivibrator: Analysis and Design of Collector Coupled Astable Multivibrator, Application of Astable Multivibrator as a Voltage to Frequency Converter.

UNIT-V: VOLTAGE TIME BASE GENERATORS

General features of a time base signal, Methods of generating time base waveform - Exponential Sweep Circuits, constant current bias circuit, Negative Resistance Switches, basic principles in Miller and Bootstrap time base generators, Transistor Miller time base generator, Transistor Bootstrap time basegenerator.

Learning Resources:

Text Books:

1.Millman J., Taub H. and Mothiki S., Rao Prakash- "Pulse, Digital and Switching Waveforms", 2Ed.,2008,McGraw Hill.

2.Bell David A.- "Pulse Switching and Digital Circuits", 5th edition 2015, OXFORD University Press

References:

1. Rao Venkata K, Sudha Rama K, Rao Manmadha G- "Pulse and Digital Circuits", Pearson,2010

2. Kumar Anand A.- "Pulse and Digital Circuits", 2005, PHI.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATIONS ENGINEERING**

Digital Image and Video Processing

(Professional Elective)

SYLLABUS FOR B.TECH

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC5T4B**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
Students will gain knowledge on DigitalImage and Video Processing techniques.	On completion of the course, studentswill be able to 1. Describe the basic concepts of Image Processing 2. Apply spatial and Frequency transform domain techniques to process images 3. Analyze different color modeling and restoration techniques 4. Analyze different morphological Image processing Techniques. 5. To understand the Basic Steps of Video Processing

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3												1	
CO2	3	2		2				1					2	
CO3	3	2	2										2	
CO4	2	2										2		
CO5	2				1									

UNIT - I:

Fundamentals of Image Processing and Image Transforms:- Introduction to digital image processing, Fundamental steps in digital image processing, components of an image processing system, Image sensing and acquisition, Representing digital images, Some basic relationships between pixels

Need for Image transforms, DFT with one variable and two variables, Properties of 2D Discrete Fourier transform, Basics of intensity transformations and spatial filtering.

UNIT - II:

Image Processing Techniques: Image Enhancement, Spatial Domain methods: Histogram Processing, Fundamentals of Spatial filtering, smoothing spatial filters, Sharpening Spatial filters.

Frequency Domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening.

Image Restoration: Degradation Model, Inverse Filtering, Least Mean Square Filters, Constrained Least Squares Restoration

UNIT - III:

Color image processing: Color fundamentals, color models, pseudo color image processing, and basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color

UNIT - IV:

Morphological Image Processing: Preliminaries, Erosion and dilation, opening and closing, The Hit or miss transformation, Some basic morphological algorithms, Gray scale morphology, Some basic gray scale morphological algorithms.

UNIT - V:

Basic Steps Of Video Processing: Analog video, Digital video, Time varying image formation model, Geometric image formation, formation, sampling of video signal.

Learning Resources:

TEXT BOOKS:

1. R. C. Gonzalez and R. E. Woods, Digital Image Processing, 3rd edition, Prentice Hall, 2008.
2. Jayaraman, S. Esakkirajan, and T. Veerakumar," Digital Image Processing", Tata McGraw-Hill Education, 2011.
3. Video Processing and Communications Yao Wang, Jorn stermann, and Ya-QinZhang Prentice Hall, 2002 (Published September 2001).

REFERENCE BOOKS:

1. Anil K.Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 9th Edition, Indian Reprint, 2002.
2. B.Chanda, D.Dutta Majumder, "Digital Image Processing and Analysis", PHI, 2009.

Online Resources:-

1. https://nptel.ac.in/courses/117/105/117105135/
2. https://nptel.ac.in/courses/117/105/117105079/

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Image and Video Processing Using Machine Learning

SYLLABUS FOR B.TECH

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	**Course Code: 22EC5T4B**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

CO-PO/PSO Mapping

COURSE OBJECTIVES	COURSE OUTCOMES
Students will gain knowledge on Image and Video Processing using Machine Learning techniques.	On completion of the course, studentswill be able to 1 Describe the basic concepts of Image Processing 2 Apply spatial and Frequency transform domain techniques to process images 3 Analyze different color modeling and restoration techniques 4. To understand the Basic Steps of Video Processing 5. To understand the Basic concepts of Machine Learning

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3												1	
CO2	3	2		2				1					2	
CO3	3	2	2										2	
CO4	2	2										2		
CO5	2				1									

Syllabus

UNIT - I:

Fundamentals of Image Processing and Image Transforms:- Introduction to digital image processing, Fundamental steps in digital image processing, components of an image processing system, Image sensing and acquisition, Representing digital images, Some basic relationships between pixels

Need for Image transforms, DFT with one variable and two variables, Properties of 2D Discrete Fourier transform, Basics of intensity transformations and spatial filtering.

UNIT - II:

Image Processing Techniques: Image Enhancement, Spatial Domain methods: Histogram Processing, Fundamentals of Spatial filtering, smoothing spatial filters, Sharpening Spatial filters.

Frequency Domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening. Image Restoration: Degradation Model, Inverse Filtering, Least Mean Square Filters, Constrained Least Squares Restoration

UNIT - III:

Color image processing: Color fundamentals, color models, pseudo color image processing, and basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color

UNIT - IV:

Basic Steps Of Video Processing: Analog video, Digital video, Time varying image formation model, Geometric image formation, formation, sampling of video signal

UNIT - V:

Introduction to Machine learning: History of Machine Learning, Types of Machine Learning, Applications of Machine Learning, Supervised Learning: Linear Regression, Logistic Regression, Decision Trees, Random Forests, Support Vector Machines (SVM) Unsupervised Learning: K-means clustering, Hierarchical Clustering Future of Machine Learning

Learning Resources:

TEXT BOOKS:

1. R. C. Gonzalez and R. E. Woods, Digital Image Processing, 3rd edition, Prentice Hall, 2008.
2. Jayaraman, S. Esakkirajan, and T. Veerakumar," Digital Image Processing", Tata McGraw-Hill Education, 2011.
3. Video Processing and Communications Yao Wang, Jorn stermann, and Ya-QinZhang Prentice Hall, 2002 (Published September 2001).

REFERENCE BOOKS:

1. Anil K.Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 9th Edition, Indian Reprint, 2002.
2. B.Chanda, D.Dutta Majumder, "Digital Image Processing and Analysis", PHI, 2009..
3.Bhagirath Bhatt,Anjali Sandep Gaikwad, G uganya "The Fundamentals of Machine Learning " Lap Lambert Academic Publicating

Online Resources:-

1. https://nptel.ac.in/courses/117/105/117105135/
2. https://nptel.ac.in/courses/117/105/117105079/

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Microprocessors and Microcontrollers Lab

SYLLABUS FOR B.TECH VI – SEMESTER

L:T:P (Hrs./week): 0:0:3	SEE Marks : 35	Course Code: **22ET5L1**
Credits : 1.5	CIE Marks : 15	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To enable the students with 8086µp 2. 8051µc based programming with built in peripheral 3. MCU IDE 8051 Assembly Language programming	On completion of the course, students will be able to 1. Apply knowledge in writing the programs using MASM assembler tool for 8086 Microprocessor. 2. Interface on chip peripherals of 8051µc 3. Execute parallel and serial communication using 8051.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2			1										
CO2	2	2			2										
CO3	2	2	1		2								1		
CO4	2	2	1		2							1	1		

PART- A: (Minimum of 5 Experiments has to be performed)

8086 Assembly Language Programming using Assembler Directives

1. Sorting.
2. Multi byte addition/subtraction
3. Sum of squares/cubes of a given n-numbers
4. Addition of n-BCD numbers
5. Factorial of given n-numbers

6. Multiplication and Division operations
7. Stack operations
8. BCD to Seven segment display CODES

PART- B: (Minimum of 3 Experiments has to be performed)
8086 Interfacing

1. Interfacing Stepper motor
2. A/D Interface through Intel 8255
3. D/A Interface through Intel 8255
4. Interfacing of Keyboard Display Controller using Intel 8279
5. Hardware/Software Interrupt Application
6. Generation of waveforms using Intel 8253/8254

PART- C: (Minimum of 3 Experiments has to be performed)
MCU IDE 8051 Assembly Language Programs

1. Finding number of 1's and number of 0's in a given 8-bit number
2. Addition of even numbers from a given array
3. Ascending / Descending order
4. Average of n-numbers

Equipment Required:

1. Regulated Power supplies
2. Analog/Digital Storage Oscilloscopes
3. 8086 Microprocessor kits
4. 8051 microcontroller kits
5. ADC module
6. DAC module
7. Stepper motor module
8. Keyboard module
9. LED, 7-Segemt Units
10. Digital Multi meters
11. ROM/RAM Interface module
12. Bread Board etc.

VLSI FRONT-END DESIGN LAB (23EV5L2)

1. Design Standard Cells Using Verilog HDL.
2. Write Verilog code for any Boolean expression.
3. Design of Full Adder using Half Adder in Verilog HDL.
4. Implement $2^n \times n$ encoder using Verilog HDL.
5. Write Verilog Code to implement 3-input combinational logic using 4x1 Multiplexer.
6. Design 4-bit even parity generator and checker logic using Verilog HDL.
7. Write Verilog Code to implement 7-segment display.
8. Write Verilog Code to implement "D" and "T" flip-flop using "JK" flip-flop.
9. Design 3-bit Random number generator using Verilog HDL.
10. Design Gated Clock 4-bit Up/down Synchronous and Asynchronous counter using Verilog Code.

Add-on experiments:

1. Implement SRAM cell using Verilog HDL
2. Implement Moore Sequence Detector Using Verilog Code.
3. Implement Mealy Sequence Generator Using Verilog Code.

With effect from the academic year 2023-24

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Constitution of INDIA

SYLLABUS FOR B.TECH V SEMESTER

L:T:P (Hrs./week): 2:0:0	SEE Marks : 00	Course Code: **22EC5MC1**
Credits : 2	CIE Marks : 00	Duration of SEE : 0 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective 2 To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism 3 To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution	On completion of the course, students will be able to 1 Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics 2 Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India. 3 Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution. 4 Discuss the passage of the Hindu Code Bill of 1956

UNIT-I :

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working), **Philosophy of the Indian Constitution:** Preamble**,** Salient Features

UNIT-II:

Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:

Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy

UNIT-V:

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women

LEARNING RESOURCES

Text Books:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

(VLSI DESIGN AND TECHNOLOGY)

Low Power VLSI Design

SYLLABUS FOR B.TECH VI – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EV6T1**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1. To acquire knowledge of powerdissipation in VLSI circuits. 2. Apply low power techniques in VLSIcircuits.	1. Understand the Fundamentals of Low Power VLSI Design. 2. Apply different circuit techniques to manage the leakage currents 3. Apply the knowledge of architectural approaches. 4. Analyze and Design Low-Voltage Low-Power combinational circuits. 5. Analyze the functionality of Low- voltage low -power memories

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2				2					2			2	
CO2	2		2		2					2			2	
CO3	2				2					2			2	
CO4		3			3					3			3	
CO5		2			2					2			2	

UNIT - I: Fundamentals of Low Power VLSI Design

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II: Low-Power Design Approaches

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches – System Level Measures, Circuit Level Measures and Mask level Measures.

UNIT - III: Low-Voltage Low-Power Adders

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT - IV: Low-Voltage Low-Power Multipliers

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V: Low-Voltage Low-Power Memories

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley.
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI DESIGN & TECHNOLOGY)

EMBEDDED SYSTEMS

SYLLABUS FOR B. TECH VI – SEMESTER

L: T: P (Hrs./week): 3:0:0	SEE Marks: 70	Course Code: **22EV6T2**
Credits: 3	CIE Marks: 30	Duration of SEE: 3 Hours

COURSE OBJECTIVES
1. Understand the basics of an embedded system.
2. To learn the design process of embedded system applications.
3. To understands the RTOS and inter-process communication.
4. To understand different communication interfaces.
5. Develop familiarity with tools used to develop in an embedded environment

COURSE OUTCOMES: On completion of the course, students will be able to	
CO 1	Understand the basic concepts of an embedded system and able to know an embedded system design approach to perform a specific function.
CO 2	Distinguish all communication devices in embedded system, other peripheral device.
CO 3	Distinguish concepts of C versus embedded C and compiler versus cross-compiler.
CO 4	Choose an operating system, and learn how to choose an RTOS
CO 5	Understand how to integrate hardware and firmware of an embedded system using real time operating system.

CO-PO/PSO Mapping:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1		3		2								2	3	
CO 2		2	3	3								2	3	
CO 3		2	3	3	3							2	3	3
CO 4		2	2	3								2	3	3
CO 5			3	2	3							2	3	3

UNIT-I:

Introduction: Embedded System-Definition, history of embedded systems, classification of embedded systems, major application areas of embedded systems, purpose of embedded systems, the typical embedded system-core of the embedded system, Memory, Sensors and Actuators, Communication Interface, Embedded firmware, Characteristics of an embedded system, Quality attributes of embedded systems, Application-specific and Domain-Specific examples of an embedded system.

UNIT-II:

Embedded Hardware Design: Analog and digital electronic components, I/O types and examples, Serial communication devices, Parallel device ports, Wireless devices, Timer and counting devices, Watchdog timer, Real time clock.

UNIT – III:

Embedded Firmware Design: Embedded Firmware design approaches, Embedded Firmware development languages, ISR concept, Interrupt sources, Interrupt servicing mechanism, Multiple interrupts, DMA, Device driver programming, Concepts of C versus Embedded C and Compiler versus Cross-compiler.

UNIT – IV:

Real Time Operating System: Operating system basics, Types of operating systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Threads, Processes and Scheduling, Task Scheduling, Communication, Synchronization, Device Drivers, how to choose an RTOS.

UNIT – V:

Embedded System Development: The Integrated Development Environment (IDE), Types of files generated on cross-compilation, Dissembler/De-compiler, Simulators, Emulators and Debugging, Target hardware debugging, Boundary Scan, Embedded Software development process and tools.

Case study-typical embedded system design flow with an example.

TEXT BOOK (S):

1. Embedded Systems Architecture by Tammy Noergaard, Elsevier Publications, 2005

2. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley Publications.

REFERENCE (S):

1. Embedding system building blocks By Labrosse, CMP publishers.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**
(VLSI Design and Technology)

CMOS Mixed Signal Circuit Design

SYLLABUS FOR B.TECH VI – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EV6T3**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

UNIT I - PHASE LOCKED LOOP

Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL.

UNIT II - SAMPLING CIRCUITS

Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures- Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

UNIT III- D/A CONVERTER ARCHITECTURES

Input/output characteristics of an ideal D/A converter, , performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, , switching functions to generate an analog output corresponding to a digital input. Resistor-Ladder architectures, Current steering architectures

UNIT IV - A/D CONVERTER ARCHITECTURES

Input/output characteristics and quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures and interleaved architectures.

UNIT V - INTEGRATOR BASED FILTERS

Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-c integrator and discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (ECE)						
		Regulation : AR-22						
Subject Code	**22EC6T4B**	Hours / Week			Credit	Maximum Marks		
Subject	**DIGITAL IC DESIGN**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**III B Tech II Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge of Analog Electronics, VLSI							
Objective	To understand the MOS Design.							
	To study Combinational MOS Logic Circuits and Sequential MOS Logic Circuits.							
	To motivate the graduate students to design and to develop the Digital Integreated Circuits for different Applications							
Outcome	**At the end of this course the student can able to:**							
	Design basic CMOS inverter.							
	Analyze the concept of Combinational & Sequential MOS circuits.							
	Design dynamic logic circuits.							
	Understand various interconnect techniques							

UNIT – I: MOS Design

Basic Electrical Properties of MOS circuits, MOS transistor threshold voltage, MOS switch and inverter, sheet resistance and area capacitances of layers, wiring capacitances; Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, CMOS Inverter logic.

UNIT – II: COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT – III: SEQUENTIAL MOS LOGIC CIRCUITS

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip flop. Dynamic, Short Circuit and Leakage power – Stacking Effect, Asymmetric gate, Skewed gates, Multipliers – Signed and Unsigned arithmetic, Carry Save Multiplier implementation

UNIT – IV: DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits. Gate sizing and Buffering

UNIT – V: SEMICONDUCTOR MEMORIES

Memory Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

LEARNING RESOURCES

Text Books:

1. Rabaey Jan M., Chandrakasan Anantha, Nikolic Borivoje-"Digital Integrated Circuits – A Design Perspective"- 2nd Ed., PHI.
2. Martin Ken-"Digital Integrated Circuit Design", Oxford University Press, 2011.

References:

1. Kang Sung-Mo, Leblebici Yusuf-"CMOS Digital Integrated Circuits Analysis and Design" – TMH, 3rd Ed., 2011.
2. Weste Neil H.E, Harris David, Banerjee Ayan-"CMOS VLSI Design"-3rd Edition, Pearson

Note: The Question paper shall have **two** sections:

- **Section A** shall consist of one question with 5 sub-questions of two (02) marks each.
- **Section B** shall consist of five questions with internal choice of ten (10) marks each, out of which five questions are required to be attempted by the candidate.

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Global Positioning System

(Professional Elective-I)

SYLLABUS FOR B.TECH VI – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC6T1C**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To study basics of mathematics and science related to GNSSconstellations 2 To understand the different coordinates for representation user position. 3 To study the different errors of GPS 4 To understand the GPS data formatsfor use of different applications 5 To acquire the knowledge of augmentation systems.	On completion of the course, students will be able to 1 Apply the knowledge of basic mathematics and science to understand the different GNSS constellations 2 Use of different coordinate systems used in user position estimation 3 Identifying the various errors of GPS. 4 Interpret the GPS data for different applications. 5 Importance of augmentation systems in various diversified applications.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2		2										2	
CO2	3	2		2										2	
CO3	3	2				2	2							2	
CO4	3					2	2					2		2	
CO5	3					2	2							2	

UNIT - I :

GPS Fundamentals: GPS Applications , GPS Constellation, Principle of operation, GPS Orbits, Orbital mechanics and satellite position determination, Time references, Geometric Dilution of Precision: Geometrical dilution of Precision, Veritical dilution of precision, Position dilution of precision.

UNIT - II :

Coordinate Systems and errors: Geometry of ellipsoid, geodeticreference system. Geoid, Ellipsoid, Global and Regional datum, World

geodetic system- 84, Different coordinate systems, Various error sourcesin GPS: Satellite and receiver clock errors, Ephemeris error, Atmospheric errors, Receiver measurement noise and User Equivalent Range Error.

UNIT - III :

GPS measurements: GPS signal structure, C/A and P-codes, Code and carrier phase measurements, position estimation with pseudo range measurements, Spoofing and anti spoofing, GPS navigation and observation data formats.

UNIT - IV :

GPS Augmentation systems: Code-based and carrier based Differential GPS(DGPS) Techniques, DGPS errors, Wide area augmentation system-architecture, GAGAN, Local area augmentation system concept.

UNIT - V :

GPS Modernization and other satellite navigation systems: Future GPS satellites, New signals and their benefits, Hardware and Software improvements, GPS integration – GPS/Geo Information System, GPS/Inertial Navigation Systedm, GPS/pseudolite, GPS/cellular, GLONASS,Galileo System.

Learning Resources:

1 Pratap Misra and Per Enge, “Global Positioning System Signals, Measurement, and Performance,” Ganga- Jamuna Press, 2/e, Massachusetts, 2010.
2 G.S.Rao, Global Navigation Satellite Systems, Tata Mc Graw-Hill, 2010.
3 Satheesh Gopi, “Global positioning system: Principles and Application", TMH, 2005.
4 B.Hofmann-Wellenhof, H.Lichtenegger, and J.Collins, “GPS Theory and Practice,” Springer Verlog, 2008.
5 Bradford W.Parkinson and James J. Spilker, “Global Positioning System: Theory and Application,” Vol.II, American Institution of Aeronautices and Astronautics Inc., Washington, 1996.
6 https://nptel.ac.in/syllabus/105107062/

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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

DSP Processors and Architectures

(Professional Elective-I)

SYLLABUS FOR B.TECH VI – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC6T2E**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To give an exposure to the fixed point point DSP architectures and toimplement various signalprocessing algorithms usingTI DSPs.	On completion of the course, students will be ableto 1 Differentiate between DSP Processors andGeneral Purpose processors. 2 Apply different number formats on DSP processors 3 Understand the architecture details of fixedpoint & floating point DSPs. 4 Illustrate the features of on-chip peripheralsand its interfacing with DSP processors. 5 Design and implement signal processing algorithms on DSP processors.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	2													1
CO2	2	2													1
CO3	1	2	1												1
CO4	1	2	2	1											2
CO5	1	2	3	2	1										3

UNIT - I : Number Format Representation and Source of Errors

Introduction, Digital signal processing system, Differences between DSP and other micro processor architectures. Fixed point, Floating point and block Floating point formats, IEEE-754 Floating point, Dynamic range and precision, Sources of error in DSP implementations, A/D Conversion errors, D/A Conversion Errors, Q-notation.

UNIT - II : Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Special addressing modes, Address Generation Unit, Programmability and Program Execution, Speed Issues, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects.

UNIT - III : Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control,TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT - IV : Floating point DSPs

Types of Floating point DSPs, Features of TMS320C67XX Processors, Architecture of 'C67X Processor-CPU, General Purpose Registers files, Functional Units and Operation, Data paths, Control Register File, Addressing modes-Register, Linear & Circular addressing modes, Instructions set-Fixed and Floating point instructions, Pipelining and on- chip peripherals.

UNIT - V : Implementations of Basic DSP Algorithms &Interfacing of 'C54xx

FIR Filters, IIR Filters, Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example, An Image Processing System.

Learning Resource:

1. Avtar Singh, S. Srinivasan "Digital Signal Processing Implementations: Using DSP Microprocessors--With Examples from TMS320C54xx", Cengage Learning (2004)
2. B. Venkataramani, M. Bhaskar, "Digital Signal Processors, Architecture Programming and Applications", Tata Mc Graw Hill, 2013.
3. Lapsley et al. "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.
4. Rulph Chassaing, "Digital Signal Processing and Applications with the C6713 and C6416 DSK", John wiley & sons, 2005.
5. Digital Signal Processing: A practical approach, Ifeachor E. C., Jervis B. W Pearson Education, PHI/ 2002
6. "Architectures for Digital Signal Processing", Peter Pirsch John Weily, 2007.
7. Jonatham Stein, "Digital Signal Processing", John Wiley, 2005.
8. https://nptel.ac.in/courses/108102045/8

IC APPLICATIONS

Course Code: 22EC6T2
REGULATIONS: AR-22

L	T	P	C
3	0	0	3

ABOUT THE COURSE:

The objective of this course is to impart thorough understanding of operational amplifiers. After completing this course, the students would be able to design and implement various signal conditioning operations involved in instrumentation, signal processing and communication systems.

PREREQUISITES: Electronic Devices and Circuits, Basic Circuit Theory

INDUSTRY SUPPORT: All Analog VLSI industries

COURSE OUTCOMES: At the end of the Course the student shall be able to

CO1 Understand the basic building blocks of Op-Amp.
CO2 Illustrate DC and AC performance characteristics of Op-Amp.
CO3 Analyze linear and non-linear applications of Op-Amp.
CO4 Analyze the operation & characteristics of data converters.
CO5 Examine various 74XX ICs.

UNIT-I 12 Lectures

OPERATIONAL AMPLIFIER

Block diagram of Op-Amp, equivalent circuit, Op-Amp Characteristics (ideal and practical) – DC and AC Characteristics, open and closed loop configurations- Inverting, Non-Inverting, Differential Amplifier.

Learning outcomes: At the end of this unit, the student will be able to

1. understand ideal and practical Op-Amps (L2)
2. understand internal blocks and characteristics of Op-Amp (L2)
3. understand performance of Op-Amp in open loop and closed loop configurations (L2)

UNIT-II 12 Lectures

APPLICATIONS OF OP-AMP

Summing, scaling and averaging amplifiers, V-I and I-V converters, Differentiators and Integrators, Comparators, Schmitt Trigger, ***Waveform Generators:*** Triangular and Square wave, ***Active filters:*** Design of First order active Low-pass and high pass filters, Band pass, Band stop and All Pass Filters.

Learning outcomes: At the end of this unit, the student will be able to

1. illustrate the amplifiers using Op-Amp (L3)
2. demonstrate waveform generators using Op-Amp (L3)
3. determine the output equations for each application of an Op-Amp (L3)

UNIT-III 14 Lectures

IC APPLICATIONS

Specialized IC applications: ***555 Timer:*** Block Schematic, Functional Diagram, Description of Individual Blocks & Applications, Monostable and Astable Operations, Introduction to VCO and PLL. ***Voltage Regulators:*** Introduction, IC voltage regulators, 723 general purpose regulators.

Learning outcomes: At the end of this unit, the student will be able to

1. understand the operation of Op-Amp based filters (L2)
2. describe internal circuit operation of 555 timer (L2)
3. Demonstrate voltage regulator using Op-Amp. (L3)

UNIT-IV 10 Lectures

DATA CONVERTERS

Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Different Types of ADCs - Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC.

Learning outcomes: At the end of this unit, the student will be able to

1. explain operation principles of different A/D & D/A converters (L2)
2. demonstrate different types of A /D & D/A converter circuits (L3)
3. evaluate ADC & DAC specifications to select the right converter for an application (L4)

UNIT-V 12 Lectures

COMBINATIONAL & SEQUENTIAL LOGIC DESIGN

Combinational Logic Design: Decoder(74x138), Priority Encoder(74x148), Multiplexer(74x151), Sequential Logic Design: D flip-flop (IC7474), JK Flip-flop(IC7476), shift register using IC7474, Universal shift Register(IC74X194), synchronous counters using flip-flops, Decade counter using IC 7476 .

Learning outcomes: At the end of this unit, the student will be able to

1. describe internal circuit operation of different Combinational I Cs (L2)
2. demonstrate Sequential circuits using 74XX ICs (L3)
3. describe Flip-flops & their conversions (L2)

TEXT BOOKS:

1. Ramakanth A. Gayakwad, *Op-Amps & Linear ICs* , 4th Edition , Pearson, 2017.
2. Wakerly J.F. *Digital Design: Principles and Practices,* 4th Edition, Pearson India, 2008.

REFERENCES:

1. D. Roy Choudhury, *Linear Integrated Circuits*, 2nd Edition, New Age International Private Limited, 2003.
2. R. P. Jain, *Modern Digital Electronics*, McGraw Hill Education (India Private Limited), 4th edition, 2012.
3. Sergio Franco, *Design with Operational Amplifiers & Analog Integrated Circuits*, 3rd edition, McGraw Hill, 1988.
4. Gray and Meyer, *Analysis and Design of Analog Integrated Circuits* , Wiley International, 2005.

SUBJECT EXPERT	HEAD OF THE DEPARTMENT	BOS MEMBER-1	BOS MEMBER-2

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY
(AUTONOMOUS)
ACCREDITED BY NAAC WITH 'A' GRADE
PARITALA, KANCHIKACHERLA–521180

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI Design and Technology)

Backend VLSI Design Lab

SYLLABUS FOR B.TECH VI SEMESTER

L:T:P(Hrs./week):0:0:3	SEE Marks:35	Course Code:**22EV6L1**
Credits:1.5	CIE Marks:15	Duration of SEE:3Hours

COURSEOBJECTIVES	COURSEOUTCOMES
1. To perform VLSI design of CMOS circuits using EDA Tools.	On completion of the course, students will be able to 1. Demonstrate the knowledge of digital circuit design flow. 2. Analyse the process of simulation of combinational sequential circuits. 3. Validate and demonstrate the results of digital circuits.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2		2		3								3		
CO2	1	2			2								1		
CO3	1	2	1		3								2		

List of Experiments:

1. Design and Implementation of Universal Gates.
2. Design and Implementation of CMOS Inverter.
3. Design and Implementation of Full Adder.
4. Design and Implementation of Full Subtractor.
5. Design and Implementation of Decoder.
6. Design and Implementation of RS-Latch.
7. Design and Implementation of D-Latch.
8. Design and Implementation asynchronous counter.
9. Design and Implementation SRAM cell.
10. Design and Implementation of ring oscillator

Additional Experiments:

1. Design and Implementation of differential amplifier
2. Design and Implementation of R-2RLadder DAC.

Software Required:

1. Mentor Graphics Software/Equivalent Industry Standard Software.
2. Personal computer system with necessary software to run the programs and to implement.

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY

(AUTONOMOUS)

PARITALA, KANCHIKACHERLA–521180

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CMOS Mixed Signal Circuit Design Lab

SYLLABUS FOR B.TECH VI SEMESTER

L:T:P(Hrs./week):0:0:3	SEE Marks:35	Course Code:**22EVT6L3**
Credits:1.5	CIE Marks:15	Duration of SEE:3Hours

COURSEOBJECTIVES	COURSEOUTCOMES
1. To perform VLSI design of CMOS circuits using EDA Tools.	On completion of the course, students will be able to 1. Demonstrate the knowledge of digital circuit design flow. 2. Analyse the process of simulation of combinational sequential circuits. 3. Validate and demonstrate the results of digital circuits.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2		2		3								3		
CO2	1	2			2								1		
CO3	1	2	1		3								2		

List of Experiments:

1. Design and Implement the **NAND & NOR Logic Gates** in Tanner EDA Tools V16.3
2. Design and Implement the **AND & OR Logic Gates** in Tanner EDA Tools V16.3
3. Design and Implement the **Ex-OR & Ex-NOR Logic Gates** in Tanner EDA Tools V16.3
4. Design and Implement the **Half-Adder** in Tanner EDA Tools V16.3
5. Design and Implement the **Full-Adder** in Tanner EDA Tools V16.3
6. Design and Implement the **D-Flipflop** in Tanner EDA Tools V16.3
7. Design and Implement the **Current Mirror** in Tanner EDA Tools V16.3
8. Design and Implement the **Differential amplifier** in Tanner EDA Tools V16.3
9. Design and Implement the **Operational Amplifier** in Tanner EDA Tools V16.3
10. Design and Implement the **Trans-Conductance Amplifier** in Tanner EDA Tools V16.3

Additional Experiments:

1. Design and Implementation of **Full-Subtractor.**
2. Design and Implementation of **R-2RLadder DAC**.

Software Required:

1. Tanner EDA Tools software Version16.3(S-Edit, T-Edit & W-Edit).
2. Personal computer system with necessary software to run the programs and to implement.

With effect from the academic year 2025-26

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY
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DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

IOT Programming Lab

SYLLABUS FOR B.TECH IV – SEMESTER

L:T:P (Hrs./week): 0:0:3	SEE Marks : 35	Course Code: **22EV6L3**
Credits : 1.5	CIE Marks : 15	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
To Prepare the students to familiarize students with Arduino as IDE, programming language & platform	1. Perform basic programming on electronic components like LED, LCD etc. 2. Mesure rotation and temperature measument 3. Design security system for different applications. 4. Measure soil moisture control.

LIST OF EXPERIMENT (MINIMUM 12 EXPERIMENT)

CYCLE - I Experiments

1. Blinking LED
2. LED BLINKING 10TIMES
3. DIRECTION OF THE LIGHT USING PHOTO RESISTER
4. INTERFACING SERVO MOTOR WITH ARDUINO
5. RELAY CONTROL

CYCLE - II Experiments

6. **16X2 LCD DISPLAY**
7. **VOICE OPERATED ON/OFF CONTROL CIRCUIT**
8. **ULTRASONIC DISTANCE MEASUREMENT**
9. **SOIL MOISTURE CONTROL**
10. **DRUNK & DRIVE DETECTION**
11. **TEMPERATURE & HUMIDITY MESUREMENT**
12. **DIRECTION CONTROL OF THE DC MOTOR USING ARDUINO**
13. **INTERFACE PIR SENSOR USING ARDUINO**

New / Additional experiments planned

1. LED Blinking of 25 times
2. Theft Alarm Circuit
3. IoT based Light Monitoring System
4. GSM pollution monitoring
5. Thermistor

Equipments

1. Computer
2. ARDUINO IDE version 2.3.3

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (EVT)						
		Regulation : AR-22						
Subject Code	**22EV7T1A**	**Hours / Week**			**Credit**	**Maximum Marks**		
Subject	**FIELD PROGRAMMABLE GATE ARRAY (FPGA) ARCHITECTURE**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**IV B Tech I Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge of Communication and Multiplexing Techniques							
Objectives	To familiarize the students with the architectural aspects of FPGA's and testing technologies of FPGA's.							
Outcomes	**At the end of this course the student can able to:**							
	Differentiate between ROM, PAL, PLA, SPLD, CPLD, and FPGA.							
	Apply the working of building blocks of FPGA to compare area and power efficiency.							
	Compare the features of Various FPGAs in terms of their Architecture, Configurable logic block.							
	Gain knowledge on placement and routing algorithms adopted in FPGAs.							
	Test a particular PLD using various techniques like design validation, Timing verification.							

UNIT – I: INTRODUCTION TO PLD'S AND PGA'S

Memory- Read-only memory, read/write memory - SRAM and DRAM. Programmable Logic Devices-PLAs, PALs and their applications; Sequential PLDs and their applications; State- machine design with sequential PLDs; Programmable gate arrays (pgas), Introduction to field programmable gate arrays (FPGAs),design flow using FPGA, programming technologies.

UNIT – II: FPGA ARCHITECTURAL ASPECTS

Field Programmable Gate Arrays: Organization of FPGAs, Programmable Logic Block Architectures, Programmable Interconnect, Programmable I/O blocksin FPGAs, Dedicated Specialized Components of FPGAs

Applications of FPGAs: Logic Block Architectures: Logic block functionality versus area-efficiency, Logic block area and routing model, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT – III: FPGA ARCHITECTURES AND COMPARISON

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC-4000, vertex-II FPGA's, XILINX SPARTAN-II, Alteras Act-1, Act-2, Act-3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT – IV: PLACEMENT AND ROUTINGALGORITHM IN FPGA ARCHITECTURES

PLACEMENT: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing.

ROUTING: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT – V: TESTING METHODS IN FPGA ARCHITECTURES

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps. Verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, and programmability failures.

LEARNING RESOURCES

Text Books:

1. S. Brown, R. Francis, J. Rose, Z.Vransic, "Field Programmable Gate array", BSP,2007
2. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.

References:

1. Spartan-3A/3AN FPGA Starter Kit Board User Guide, 2010
2. S. Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
3. https://nptel.ac.in/syllabus/117108040/prof.Kuruvilla Varghese IISC Banglore

Note: The Question paper shall have **two** sections:

- **Section A** shall consist of one question with 5 sub-questions of two (02) marks each.
- **Section B** shall consist of five questions with internal choice of twelve (12) marks each, out of which five questions are required to be attempted by the candidate.

Course Code 22EC7T2A	Wireless Mobile Communication	L	T	P	C
	Maximum expected contact hours : **64**	**3**	**1**	**--**	**3**
	Prerequisites : Fundamentals of ***Communication Systems***				

PURPOSE: students will understand the mobile technologies and communications	
INSTRUCTIONAL COURSE OBJECTIVES	
1	To understand the basic cellular system concepts
2	To have an insight into the various propagation models and the speech coders used in mobile communication.
3	To understand the multiple access techniques and inte rference reduction techniques in mobile communication.
COURSE OUTCOMES :	
1	Discuss cellular radio concepts.
2	Identify various propagation effects
3	Acquire knowledge of mobile system specifications
4	Classify multiple access techniques in mobile communication.
5	Analyze various methodologies to improve the cellular capacity.

UNIT I: BASICS OF ANALOG CELLULAR SYSTEMS:

CELLULAR MOBILE RADIO SYSTEMS: Introduction to Cellular Mobile System, Performance criteria, uniqueness of mobile radio environment, operation of cellular systems, Hexagonal shaped cells.

ELEMENTS OF CELLULAR RADIO SYSTEM DESIGN:

General description of the problem, concept of frequency channels, Co-channel Interference Reduction Factor, desired C/I from a normal case in a Omni directional Antenna system, Cell splitting, consideration of the components of Cellular system.

UNIT II: CHANNEL INTERFERENCE AND CELL COVERAGE

INTERFERENCE: Introduction to Co -Channel Interference, real time Co-Channel interference, Adjascent-Channel measurement, Antenna parameters and their effects, non co-channel interference- different types.

CELL COVERAGE FOR SIGNAL AND TRAFFIC: Signal reflections in flat and hilly terrain, effect of human made structures, phase difference between direct and reflected paths, constant standard deviation, straight line path loss slope, and near and long distance propagation antenna height gain, form of a point to point model.

UNIT III: HAND-OFF AND BASICS OF DIGITAL CELLULAR SYSTEMS

HAND-OFF: Numbering and grouping, setup access and paging channels channel assignments to cell sites and mobile units, channel sharing and borrowing, Handoff, types of handoff , dropped calls and cell splitting.

2G-NETWORK: GSM, GSM Architecture, GSM channel and channel modes, multiple access schemes,channel coding and Interleaving

UNIT IV: DIGITAL CELLULAR SYSTEMS APPLICATION

CDMA: Terms of CDMA, Modulation Characteristics, Call Processing

GPRS: GPRS, GPRS architecture, GPRS network architecture, GPRS transmission plane & signaling plane, GPRS traffic performance.

UNIT –V: B2G SYSTEMS WITH 3G TECHNOLOGY

B2G SYSTEMS: EDGE: network architecture, network control, HSCSD: iDEN.

3G Technology: UMTS architecture, description, WCDMA, CDMA2000 - architecture, bandwidth requirement, characteristics

TEXTBOOKS:

1. Mobile Cellular Telecommunications – W.C.Y. Lee, Tata McGraw Hill, 2rd Edn., 2006.
2. Principles of Mobile Communications – Gordon L. Stuber, Springer International 2nd Edition, 2007.

REFERENCES:

1. Wireless Communications - Theodore. S. Rapport, Pearson education, 2nd Edn., 2002.
2. Wireless and Mobile Communications – Lee McGraw Hills, 3rd Edition, 2006.
3. Mobile Cellular Communication – G Sasibhushana Rao Pearson
4. Wireless Communication and Networking – Jon W. Mark and Weihua Zhqung, PHI, 2005.
5. Wireless Communication Technology – R. Blake, Thompson Asia Pvt. Ltd., 2004.

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (EVT & ECA)						
		Regulation : AR-22						
Subject Code	**22EC7T3E**	**Hours / Week**			**Credit**	**Maximum Marks**		
Subject	**IOT ARCHITECHTURE & PROTOCOL**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**VII B Tech I Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge of IOT device, architecture & communication models							
Objectives	Understand IoT applications and IoT Architectures.							
	Learn about IIoT devices and event driven analysis							
	Understand and analyze IoT.							
	Understand safety and security testing of IoT systems							
Outcomes	**At the end of this course the student can able to**							
	Demonstrate the revolution of internet in mobile and cloud.							
	Examine the architecture and operation of IoT.							
	Explore various tools and programming paradigms for IoT applications.							
	Develop an IoT prototype for real time scenario.							
	Use IoT Data Link Layer, Network Layer IoT, Transport & Session Layer Protocols							

UNIT – I: THE IOT LANDSCAPE

Definition of IoT, Applications, Architectures, Wireless Networks, Devices, Security and Privacy, Event-Driven Systems.

IoT System Architectures: Introduction, Protocols Concepts, IoT oriented Protocols, Databases, Time Bases, Security.

UNIT – II: IOT- AN ARCHITECTURAL OVERVIEW & ARCHITECTURE-STATE OF THE ART

IoT- An Architectural Overview: Building architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

IoT Architecture-State of the Art: Introduction, State of the art, Reference Model and architecture,

IoT Reference Model - IoT Reference Architecture, Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT – III: INDUSTRIAL INTERNET OF THINGS & SECURITY AND SAFETY

Introduction, Industry 4.0, Industrial Internet of Things (IIoT), IIoT Architecture, Basic Technologies, Applications and Challenges.

Security and Safety: Introduction, Systems & Security, Network Security, Generic Application Security, Application Process Security and Safety

UNIT – IV: IOT DATA LINK LAYER

IoT Data Link Layer: PHY/MAC Layer (3 GPPMTC, IEEE 802.11, IEEE 802.15),Wireless HART, Z Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH 7

UNIT – V: Network Layer Protocols & IOT Transport & Session Layer Protocols

Network Layer Protocols: Network Layer- IPv4, IPv6, 6LoWPAN, 6TiSCH, ND, DHCP, ICMP

IOT Transport Protocols: Transport Layer(TCP, MPTCP, UDP, DCCP, SCTP)- (TLS, DTLS)

IOT Session Layer Protocols: Session Layer- HTTP, CoAP

LEARNING RESOURCES

Text Books:

1. Dimitrios Serpanos, Marilyn Wol, "Internet-of-Things (IoT) Systems Architectures, Algorithms, Methodologies", ISBN 978-3-319-69714-7.
2. Danial Minoli, "Building the Internet of Things with IPv6 and M IPv6: The Evolving World of M2M Communications", ISBN: 978-1-118-47347-4, Willy Publications, 2016
3. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Aves and, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence",1st Edition, Academic Press, 2015.

References:

1. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642-19156-5e-ISBN978-3-642-19157-2, Springer, 2016.
2. N. Ida, Sensors, Actuators and Their Interfaces, Scitech Publishers, 2014.
3. Internet of Things– A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015.
4. The Internet of Things– Key applications and Protocols, Olivier Hersent, David oswarthick, Omar Elloumi and Wiley, 2012

E-Resources:

1. https://sist.sathyabama.ac.in/sist_coursematerial/uploads/SCSA1408.pdf
2. https://www.studocu.com/in/document/jawaharlal-nehru-technological-university-anantapur/iot-communication-protocols/unit-iii-iot-notes/65078702

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (ECE)						
		Regulation : AR-22						
Subject Code	**22EC7T1C**	**Hours / Week**			**Credit**	**Maximum Marks**		
Subject	**OPTICAL FIBER COMMUNICATION**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**IV B Tech I Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge of Microwave Devices, Semiconductor Physics							
Objectives	The properties of optical fiber that affect the performance of a communication link and types of fiber materials with their properties and the losses occur in fibers							
	the principles of single and multi-mode optical fibers and their characteristic							
	Working of semiconductor lasers, and differentiates between direct modulation and external electro-optic modulation							
	Analyze the operation of LEDs, laser diodes, and PIN photo detectors (spectral properties, bandwidth, and circuits) and apply in optical systems							
	The models of analog and digital receivers							
Outcomes	**At the end of this course the student can able to:**							
	Use the concept of optical fiber in communication system.							
	Able to measure the power & efficiency for optical source							
	Use different types of photo detectors and optical test equipment to analyze optical fiber and light wave systems.							
	Choose the optical cables for better communication with minimum losses Design, build, and demonstrate optical fiber experiments in the laboratory							

UNIT – I: INTRODUCTION

Overview of optical fiber communication, Historical development, general system, advantages and applications of optical fiber communications, Optical fiber wave guides- Introduction, types of rays, Ray theory transmission, Total Internal Reflection, Acceptance angle, Numerical Aperture, Cylindrical fibers- Modes, V-number, Mode coupling, Step Index fibers, Graded Index fibers, Single mode fibers- Cut off wavelength, Mode Field Diameter, Effective Refractive Index, Related problems

UNIT – II: FIBER LOSSES

Fiber materials: - Glass, Halide, Active glass, Chalgenide glass, Plastic optical fibers. Signal distortion in optical fibers-Attenuation, Absorption, Scattering and Bending losses, Core and Cladding losses, Information capacity determination, Group delay, Types of Dispersion:- Material dispersion, Wave-guide dispersion, Polarization-Mode dispersion, Intermodal dispersion, Pulse broadening in Graded index fiber, Related problems

UNIT – III: OPTICAL SOURCES

Optical sources- Direct and indirect Band gap materials, LEDs, Structures, Materials, Quantum efficiency, Power, Modulation, Power bandwidth product. Injection Laser Diodes- Modes, Threshold conditions, External quantum efficiency, Laser diode rate equations, Resonant frequencies, Reliability of LED & ILD, Optical detectors- Physical principles of PIN and APD, Detector response time, Temperature effect on Avalanche gain, Comparison of Photo detectors, Related problems

UNIT – IV: FIBER CONNECTOR & OPTICAL SYSTEM DESIGN

FIBER CONNECTOR: Optical fiber Connectors-Preparation of optical fiber for connection, Connector types, lensing schemes ,Connector return loss, Fiber Splicing- Splicing techniques, Fiber misalignment and joint loss-Multimode fiber joints, single mode fiber joints

OPTICAL SYSTEM DESIGN: Point-to- point links- Component choice and considerations, Link power budget, Rise time budget with examples, Line coding in Optical links, WDM, Necessity, Principles, Measurement of Attenuation and Dispersion, Eye pattern

UNIT – V: FIBER POWER

Source to fiber power launching - Output patterns, Power coupling, Power launching, Equilibrium Numerical Aperture, Laser diode to fiber coupling, Optical receiver operation- Fundamental receiver operation, Digital signal transmission, error sources, Receiver configuration, Digital receiver performance, Probability of Error, Quantum limit, Analog receivers

LEARNING RESOURCES

Text Books:

1. Keiser Gerd- “Optical Fiber Communications”, Mc Graw-Hill International edition, 3rd Edition, 2000
2. Senior John M.- “Optical Fiber Communications”, PHI, 2nd Edition, 2002
3. Agarwal Govind P.- “Fiber Optic Communication Systems”, John Wiley, 3rd Ediition, 2004.

References:

1. Senior John M.- “Optical Fiber Communication Principles and Practice”, Pearson Publication, 3rd Edition, 2015.
2. Mynbaev D.K., Gupta S.C. and Scheiner Lowell L.- “Fiber Optic Communications”, Pearson Education,2005.
3. Gupta S.C.- “Text Book on Optical Fiber Communication and its Applications”, PHI, 2005
4. Palais Joseph C.- “Fiber Optic Communications”, 4th Edition, Pearson Education, 2004

With effect from the academic year 2022-23

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY

(AUTONOMOUS)

ACCREDITED BY NAAC WITH 'A' GRADE

PARITALA, KANCHIKACHERLA – 521180

DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Advanced Embedded Systems

(Professional Elective-V)

SYLLABUS FOR B.TECH VII – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC7T5A**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Define and classify embedded system and to interpret design process and challenges. 2 Summarize the RISC concepts and describe the ARM architecture, Interpret serial and parallel bus communication protocols. 3 Describe system design and co-design issues along with various laboratory, IDE tools and design case studies.	On completion of the course, students will be able to 1 Define embedded system & describe the embedded system product design life cycle and challenges. 2 Analyse the ARM Core embedded design and its programming model. 3 Apply knowledge to design networked embedded systems using serial, parallel and wireless communication protocols. 4 Justify the importance of hardware software co-design and models involved. 5 Acquire the knowledge of embedded IDEs to design and specify debugging techniques.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	3	3	2	2	1		1	2	1	1	2	3	3	2
CO2	2	3	3	2	2	1		1	2	1	2	2	3	2	2
CO3	2	3	3	2	3	1		1	2	1	2	2	3	3	2
CO4	2	3	3	2	2	2		1	2	1	2	2	3	3	2
CO5	2	3	3	2	3	1		1	2	1	1	2	3	3	2

UNIT – I :

Embedded System Design: Introduction, Trends, Definition, Classifications; Embedded Product Development Life Cycle. CPU selection– hardware, software, memories, and I/O. Challenges in designing Embedded System; Design Metric of Embedded System.

UNIT - II:

ARM Processor Fundamentals: Nomenclature; Core Architecture; AMBA Bus; Registers; operating modes; Pipeline; Thumb Mode; Exceptions, OBD using JTAG; Overview of ARM Assembly Instructions

(Data processing & Branching); ARM Core features Comparisons.

UNIT - III:

Embedded Networking: Traditional Networking Vs Embedded Networking; Networking through serial protocols: UART, I2C, SPI, CAN, IEEE1394 and USB; Porting of TCP/IP – Socket selection; HTTP client-server model; Design Considerations.

UNIT - IV:

Hardware Software Codesign: Comparison of Co-Design Approaches; Formulation of the HW/SW scheduling, Optimization of Design Metric: Case study of Embedded Adaptive Cruise Control Design.

Embedded Software Architectures: Round Robin, RR with Interrupt driven and Functional Queue architectures.

UNIT - V:

Embedded Development tools: Host and Target machines, Instruction packing: Big-endian ISA Vs Little Endian ISA; Intel Vs Motorola Modes.

Debugging Methods: Testing on Host–Instruction set Simulators, native tools–IDEs; cross-compilers; ICE, JTAG, laboratory tools: Multi meter, CRO, Logic Analyzer & protocol sniffers.

Learning Resource:

1 Tony Givargis Frank Vahid "Embedded System Design: A Unified Hardware/Software Introduction" Wiley Student Edition, 2006
2 Andrew Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Morgan Kaufmann Publishers In, 2004
3 Marilyn Wolf, "Computers as Components: Principles of Embedded Computing Systems Design", Elsevier; Third edition (2013)
4 MOOCs: https://nptel.ac.in/noc/individual_course.php?id=noc19-cs22

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (ECA)						
		Regulation : AR-22						
Subject Code	**22EA7T1B**	Hours / Week			Credit	Maximum Marks		
Subject	**MULTICARRIER COMMUNICATION SYSTEMS**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**IV B Tech I Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge of Communication and Multiplexing Techniques							
Objectives	To provide an overview of OFDM and wireless channel characteristics							
	To understand the basic concepts of synchronization and channel impairment in OFDM							
Outcomes	**At the end of this course the student can able to:**							
	Understand the basics of OFDM and wireless channel characteristics							
	Learn the concepts of synchronization and channel impairment in OFDM							

UNIT – I: INTRODUCTION

Multi carrier and OFDM system fundamentals, OFDM system model, Single carrier communication, Comparison with other multi carrier modulation scheme, Channel capacity

UNIT – II: SPECTRUM OF OFDM

FFT implementation, Power spectrum, Impairments of wireless channels to OFDM signals, Synchronization in OFDM, Timing and Frequency Offset in OFDM, Synchronization & system architecture

UNIT – III: OFFSET ESTIMATION & CHANNEL ESTIMATION

OFFSET ESTIMATION: Timing and Frequency Offset estimation, Pilot and Non pilot based methods, Joint Time & Frequency Offset estimation

CHANNEL ESTIMATION: Channel Estimation in OFDM systems, Differential and Coherent detection, and Pilot symbol aided estimation, Block type and Comb type pilot arrangement

UNIT – IV: MIMO CHANNEL ESTIMATION

Decision directed channel estimation, MMSE estimation using time and frequency domain, correlation, MIMO channel estimation- basic concepts, Concepts of Time and Frequency domain equalization

UNIT – V: PROPERTIES OF OFDM

Clipping in Multi carrier systems, Power amplifier non linearity, Error probability analysis, Performance in AWGN channel, PAPR properties of OFDM signals, PAPR reduction techniques with signal distortion, Techniques for distortion less PAPR reduction, Selective mapping and Optimization techniques

LEARNING RESOURCES

Text Books:

1. Stuber Y. Li. G.- "OFDM for Wireless Communication", Springer, 2006
2. Prasad R.- "OFDM for Wireless Communication", Artech House, 2006

References:

1. Bahai Ahmad R.S., Saltzberg B.R., Ergen M.- " Multi carrier Digital Communications Theory and Applications of OFDM", Second Edition, Springer

Note: The Question paper shall have **two** sections:

- **Section A** shall consist of one question with 5 sub-questions of two (02) marks each.
- **Section B** shall consist of five questions with internal choice of twelve (12) marks each, out of which five questions are required to be attempted by the candidate.

Department : *ELECTRONICS AND COMMUNICATION ENGINEERING*		Programme: B. Tech. (ECA)						
		Regulation : AR-22						
Subject Code	**22EA7T3B**	Hours / Week			Credit	Maximum Marks		
Subject	**SATELLITE COMMUNICATION**	**L**	**T**	**P**	**C**	**IM**	**EM**	**TM**
Year & Sem	**IV B Tech I Semester**	3	1	0	3	30	70	100
Prerequisite	Basic Knowledge of Communication Systems							
Objectives	Prepare students to excel in basic knowledge of satellite communication principles							
	Provide students with solid foundation in orbital mechanics and launches for the satellite communication							
	Train the students with a basic knowledge of link design of satellite with a design examples							
	Provide better understanding of multiple access systems and earth station technology							
	Prepare students with knowledge in satellite navigation and GPS & and satellite packet communications							
Outcomes	**At the end of this course the student can able to:**							
	Understand the historical background, basic concepts and frequency allocations for satellite communication							
	Exhibit orbital mechanics, launch vehicles and launchers							
	Demonstrate the design of satellite links for specified C/ N with system design examples.							
	Visualize satellite sub systems like Telemetry, tracking, command and monitoring power systems and Understand the various multiple access systems for satellite communication systems and satellite packet communications							
	Gain knowledge about satellite navigation system with GPS technology							

UNIT – I: COMMUNICATION SATELLITE

Orbit and Description: A Brief history of satellite Communication, Satellite Frequency Bands, Satellite Systems, Applications, Orbital Mechanics and Launchers: Orbital Mechanics, Look Angel Determinations, Orbital Period and Velocity, effects of Orbital Inclination, Coverage angle and slant Range, Eclipse, Orbital Perturbations, Placement of a Satellite in a Geo-Stationary orbit. Orbital Determination, Launches and Launch Vehicles, Orbital Effects in Communication Systems Performance, Future Trends of Satellite Communications

UNIT – II: SUB-SYSTEMS AND LINK DESIGN

Satellite Sub-Systems: Attitude and Orbit Control system, TT & C subsystem, Attitude Control subsystem, Power systems, Communication sub-systems, Satellite Antenna Equipment, Equipment Reliability and Space Qualification.

Satellite Link Design: Basic Transmission Theory, System Noise Temperature and G/T ratio, Basic UP/DOWN Link Analysis, Interference Analysis, Design of satellite Links for a specified C/N, (With and without frequency Re-use), Link Budget

UNIT – III: PROPAGATION EFFECTS AND MULTIPLE ACCESS

Propagation effects: Introduction, Atmospheric Absorption, Cloud Attenuation, Tropospheric and Ionospeheric Scintillation and Low angle fading, Rain induced attenuation, rain induced cross polarization interference.

Multiple Access: Frequency Division Multiple Access (FDMA) – Inter-modulation, Calculation of C/N, Time Division Multiple Access (TDMA) - Frame Structure, Burst Structure, Satellite Switched TDMA, On-board Processing,Demand Assignment Multiple Access (DAMA) – Types of Demand Assignment, Characteristics, CDMA Spread Spectrum Transmission and Reception

UNIT – IV: LEO, GEO WITH SATELLITE PACKET SYSTEMS

LOW EARTH ORBIT: Transmitters, Receivers, Antennas, Tracking Systems, Terrestrial Interface, Power Test Methods, Lower Orbit Considerations.

GEO-STATIONARY SATELLITE SYSTEMS: Orbit Considerations Coverage and Frequency Consideration, Delay and Throughput Considerations, Systems Considerations, Operational NGSO Constellation Designs

SATELLITE TRANSMISSION: Packet Communications: Message Transmission by FDMA: M/ G/1 Queue, Message Transmission by TDMA, PURE ALOHA-Satellite Packet Switching, Slotted Aloha, Packet Reservation, Tree Algorithm

UNIT – V: SATELLITE NAVIGATION AND GLOBAL POSITIONING SYSTEM

Radio and Satellite Navigation, GPS Position Location Principles, GPS Receivers and Codes, Satellite Signal Acquisition, GPS Navigation Message, GPS Signal levels, GPS Receiver Operation, GPS C\A Code Accuracy, Differential GPS

LEARNING RESOURCES

Text Books:

1. Pratt Timothy, Bostian Charles, Allnutt Jeremy- "Satellite Communications", 2nd Edition, 2003, John Wiley & Sons.
2. Pritchand Wilbur L., Nelson Robert A. and Suyderhoud Heuri G.- "Satellite Communications Engineering", 2nd Ed., Pearson Publications
3. Ha Tri.T.- "Digital Satellite Communications", 2nd Edition, 1990, Mc.Graw Hill

References:

1. Roddy Dennis- "Satellite Communications", 2nd Edition, 1996, McGraw Hill.

2. Richcharia M.- “Satellite Communications: Design Principles”, 2nd Ed., BSP, 2003.
3. Rao Raja K. N.- “Fundamentals of Satellite Communications”, PHI, 2004
4. Agarwal D.C.- “Satellite Communications”, khanna Publications,5th Edition

Note: The Question paper shall have **two** sections:

- **Section A** shall consist of one question with 5 sub-questions of two (02) marks each.
- **Section B** shall consist of five questions with internal choice of ten (10) marks each, out of which five questions are required to be attempted by the candidate.

AMRITA SAI INSTITUTE OF SCIENCE AND TECHNOLOGY

(AUTONOMOUS)

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PARITALA, KANCHIKACHERLA – 521180

DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Biomedical Signal Processing

(Professional Elective-IV)

SYLLABUS FOR B.TECH VII – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC7T4C**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 To introduce the fundamentals of probability theory and random processes with biomedical signals applications. 2 To equip students with the fundamental tools that are used to describe, analyze and process biomedical signals. 3 To acquire the knowledge on fundamental principles in the analysis and design of filters, power spectral density estimation and non-stationary signal processing techniques with cardiological and neurological signals.	On completion of the course, students will be able to 1 Apply the probability theory and random processes techniques in analyzing biological signals. 2 Determine to best class of compression techniques to use for a particular bio medical signal to compress. 3 Possess the basic mathematical, scientific and computational skills necessary to analyze and process cardiological signals as per the requirement. 4 Ability to formulate and solve basic problems in biomedical signal analysis. 5 Possess the basic mathematical, scientific and computational skills necessary to analyze and process neurological signals as per the requirement.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	3	2	2	2	2		1			1	1		2	
CO2	2	3	2	2	2	2		1			1	1		2	
CO3	2	3	2	2	2	2		1			1	1		2	
CO4	2	3	2	2	2	2		1			2	1		2	
CO5	2	3	2	2	2	2		2			1	2		2	

UNIT – I

Discrete and continuous Random variables: Probability distribution and density functions. Gaussian and Rayleigh density functions, Correlation between random variables.

Stationary random process, Ergodicity, Power spectral density and autocorrelation function of random processes. Noise power spectral density analysis, Noise bandwidth, noise figure of systems.

UNIT – II

Data Compression Techniques: Lossy and Lossless data reduction Algorithms. ECG data compression using Turning point, AZTEC, CORTES, Huffman coding, vector quantisation, DCT and the K L transform.

UNIT – III

Cardiological Signal Processing: Pre-processing. QRS Detection Methods. Rhythm analysis. Arrhythmia Detection Algorithms. Automated ECG Analysis. ECG Pattern Recognition. Heart rate variability analysis.

Adaptive Noise Cancelling: Principles of Adaptive Noise Cancelling. Adaptive Noise Cancelling with the LMS Adaptation Algorithm. Noise Cancelling Method to Enhance ECG Monitoring. Fetal ECG Monitoring.

UNIT – IV

Signal Averaging, polishing – mean and trend removal, Prony's method, Prony's Method based on the Least Squares Estimate, Linear prediction. Yule – walker (Y –W) equations, Analysis of Evoked Potentials.

UNIT-V

Neurological Signal Processing: Modelling of EEG Signals. Detection of spikes and spindles Detection of Alpha, Beta and Gamma Waves. Auto Regressive (A.R.) modelling of seizure EEG. Sleep Stage analysis. Inverse Filtering. Least squares and polynomial modelling.

Learning Resources:

1. Probability, Random Variables & Random Signal Principles – Peyton Z. Peebles, 4th ed., 2009, TMH.
2. Biomedical Signal Processing- Principles and Techniques – D.C.Reddy, 2005, TMH.
3. Digital Bio signal Processing – Weitkunat R, 1991, Elsevier.
4. Biomedical Signal Processing – Akay M, IEEE Press.
5. Biomedical Signal Processing –Vol. I Time & Frequency Analysis – Cohen.A, 1986, CRC Press.
6. Biomedical digital Signal Processing: C-Language Experiments and Laboratory Experiments, Willis J.Tompkins, PHI.
7. https://nptel.ac.in/courses/108105101/ Biomedical Signal Processing – by Prof.Sudipta Mukhopadhyay. IITKGP
8. http://www.ecdept.iitkgp.ac.in/index.php/home/faculty/smukho

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PARITALA, KANCHIKACHERLA – 521180

DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Electronic Instrumentation

(Professional Elective-I)

SYLLABUS FOR B.TECH VII – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC7T1B**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Explain basic concepts and definitions inmeasurement. 2 Elaborate discussion about the importance of signal generators and analyzers in Measurement. 3 provide a brief knowledgeof measurements and measuring instruments related to engineering	On completion of the course, students will be ableto 1 Identify different characteristics of instrumentsand errors in measurements. 2 To use modern instruments for measurements. 3 Demonstrate working principle and usage of medical instruments. 4 Modeling of various applications in virtual instrumentation. 5 Analyze various voltmeters, CRO, spectrum analyzer.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	2	3										3		
CO2		1	1										3		
CO3	2	2	3										3		
CO4	1	2	3										3		
CO5	2	2	3										3		

UNIT – I

Accuracy, Precision, Resolution and Sensitivity. Errors and their types. Standards of measurement, classification of standards, IEEE standards, Elements of ISO 9001, Quality management standards.

UNIT – II

Transducers: classification, factors for selection of a transducer, transducers for measurement of velocity, acceleration, force, radio activity, Hot wire anemometer. Passive electrical transducers- Strain gauges and strain measurement, LVDT and displacement measurement, capacitive transducer and thickness measurement. Active electrical transducers: Piezo electric, photo conductive, photo voltaic and photo emissive transducers.

UNIT – III

Characteristics of sound, pressure, power and loudness measurement. Microphones and their types. Temperature measurement, resistance wire thermometers, semiconductor thermometers and thermocouples. Humidity measurement, resistive capacitive, aluminum oxide and crystal Hygrometer types.

UNIT – IV

Block diagram, specification and design considerations of different typesof DVMs. Digital LCR meters, Spectrum analyzers. The IEEE488 or GPIB Interface and protocol.

Delayed time base oscilloscope, Digital storage oscilloscope, and mixed signal oscilloscope. Introduction to virtual instrumentation, SCADA. Data acquisition system block diagram

UNIT-V

Biomedical Instrumentation: Human physiological systems and related concepts. Bio-potential electrodes Bio-potential recorders - ECG, EEG, EMG, X- ray machines and CT scanners, magnetic resonance and imaging systems, Ultrasonic Imaging systems.

Learning Resources:

1 Albert D. Helfric, and William D. Cooper, “Modern Electronic Instrumentation and Measurement Techniques”, PHI, 2010.
2 H S Kalsi, “Electronic Instrumentation”, 3/e, TMH, 2011.
3 Nakra B.C, and Chaudhry K.K., “Instrumentation, Measurement and Analysis”, TMH, 2004
4 Khandpur. R.S., “Handbook of Bio-Medical Instrumentation”, TMH, 2003.
5 https://nptel.ac.in/courses/108105064

With effect from the academic year 2022-23

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PARITALA, KANCHIKACHERLA – 521180

DEPARTMENT OF **ELECTRONICS AND COMMUNICATION ENGINEERING**

Wireless Sensor Networks

(Professional Elective-II)

SYLLABUS FOR B.TECH VII – SEMESTER

L:T:P (Hrs./week): 3:0:0	SEE Marks : 70	Course Code: **22EC7T2C**
Credits : 3	CIE Marks : 30	Duration of SEE : 3 Hours

COURSE OBJECTIVES	COURSE OUTCOMES
1 Differentiate WSNs and mobile ad-hoc networks and illustrate the single node computational blocks and design challenges narrating WSNfundamental entities. 2 Analyze and Summarize the MAC (L-2) and Routing (L-3) protocols along with the physical transceiver radio design. 3 Describe WSN topology, localization along with existing hardware support and software simulators and programming models.	On completion of the course, students will be able to 1 Analuyze Wireless Sensor Network Characteristics and its challenges; and, differentiate WSN with other ad-hoc networks. 2 Illustrate architecture of Single WSN mote with Energy consumption mathematical models of a single mote both during the transmission and reception. 3 Apply Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks and their comparisons 4 Analyze different topology control and clustering schemes with localization concepts. 5 Describe some of the widely used WSN simulation tools and platforms with engineering case studies.

CO-PO/PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	2											2	
CO2	3	3	2											2	
CO3	3	3	2											2	
CO4	2	3	2											2	
CO5	3	3	2											2	

UNIT - I : OVERVIEW OF WIRELESS SENSOR NETWORKS

Challenges for Wireless Sensor Networks Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- Enabling Technologies for Wireless Sensor Networks

UNIT - II : ARCHITECTURES

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concept

UNIT - III : NETWORKING SENSORS

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC, Zigbee: IEEE 802.15.4 MAC Layer, The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

UNIT - IV : INFRASTRUCTURE ESTABLISHMENT

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT - V : SENSOR NETWORK PLATFORMS AND TOOLS

Operating Systems for Wireless Sensor Networks, Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms, Node-level Simulators, State-centric programming.

Learning Resource:

1. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks," John Wiley, 2005.
2. Feng Zhao and Leonidas J. Guibas, “Wireless Sensor Networks - An Information Processing Approach," Elsevier, 2007.
3. Kazem Sohraby, Daniel Minoli, and Taieb Znati, “Wireless Sensor Networks-Technology, Protocols and Applications,” John Wiley, 2007.
4. Anna Hac, “Wireless Sensor Network Designs,” John Wiley, 2003.
5. https://nptel.ac.in/courses/106105160/21

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PARITALA, KANCHIKACHERLA – 521180

DEPARTMENT OF **COMPUTER SCIENCE AND ENGINEERING**

HUMAN RESOURCE DEVELOPMENT

SYLLABUS FOR B.TECH VII– SEMESTER

L:T:P (Hrs./week): 04	SEE Marks : 70	Course Code: 20HS7T6
Credits : 3	CIE Marks : 30	Duration of SEE 3hrs

COURSE OBJECTIVES	COURSE OUTCOMES
provide a conducive environment that holistically engages students through an all–encompassing knowledge impartation and comprehensive practical applications.	HRD helps to improve the skills, knowledge, and abilities of employees, which leads to improved performance and productivity. It helps to create a positive work environment that fosters continuous learning and development
Mould students into future visionaries and management leaders that are benevolent yet efficacious, versed in the leading business and human resource practices of the world and equipped to the hilt to implement themselves and adapt to the mutable global business environment.	Students shall gain an in-depth knowledge and analytical skills which will enable them to effectively and efficiently carry out various human resource and
student will learn the importance of Coaching and performance improvement and gain knowledge of mentoring	HRD's main goal is to help employees gain knowledge, learn new concepts, and improve existing abilities. HRD's main goal is to improve the quality of the workforce by establishing an atmosphere that encourages continuous learning and mentoring
Develop managerial knowledge and strategic agility, providing students with a broader skill set and a fresh perspective and encouraging them to seek out bold, innovative solutions for today‟s business and societal challenge.	Students shall gain an in-depth knowledge and analytical skills which will enable them to effectively and efficiently carry out various human resource and organizational development operations of an organization in the emerging globalized environment
Offer a deep dive into various facets of human resources management and organizational development by integration of cross-cutting issues relevant	(HRD) Programme is mainly oriented towards professional augmentation taking place in the global as well as domestic business arena and the

to gender, environment and sustainability,	curriculum thus intends to reduce the gap between industry and academia, with the right blend of theory and practice,

UNIT-I:

Concept of HRD-objectives-Structure-Need-Scope- HRD in selected industrial organisations- significance-HRD functions-Framework-Techniques-Attributes of a HRD manager.

UNIT – II:

HRD Strategies:- An Overview - Strategies - Training and Development - Methods - Evaluation of training programmes. HRD Process Model: Methods of Implantation, Evaluation of HRD programmes .Identification of HRD needs and Design and development of HRD programmes.

UNIT – III:

HRD interventions: Mentoring for employee development: Concepts of Mentoring-Perspectives-Mentoring relationship-Outcomes of Mentoring programmes-Design and implementation of formal-mentoring programmes-Barriers to mentoring-Role of mentoring in development, understanding the role and responsibilities of mentor, mentee-Special issues in Mentoring.

UNIT – IV:

Intellectual capital (IC),: its measurement and management: Components of IC, measurement models of IC, IC index and challenges for HR

UNIT – V

Employee counselling for HRD: Overview of counselling programmes, employee assistance programme, stress management, employee wellness and health promotion. Career Planning, management, and development: Career development stages and activities, role of individual and organization in career planning, Issues in career management.

UNIT-VI

The future of HRD and HRD Ethics: Research, practice and education of HRD for innovation and talent development and management, Role of HRD in developing ethical attitude and behaviour and development, Ethical problems with HRD roles. Applications of HRD: HRD Climate, HRD for managing organizational change, HRD for Workers (blue collar employees), HRD Audit.

References:

1. Arun Monappa; PersonnelManagement;
2. Rudrabasava Raj M.N. : Dynamic Personnel Administration Management of Human Resources;
3. Udai Pareek, Human Resource Development;
4. S. Ravishankar & R.K. Mishra (Ed). : Management of Human Resources inPublic Enterprises;
5. Haribson F, Educational Planning and Human Resources Development, InternationalInstitute for Education, UNESCO,Paris;
6. Bell DJ, Planning Corporate' Manpower, Longman; 7, Walker James W'. Human Resource Planning,MGH.